From All-Si Nanowire TFETs Towards III-V TFETs

THÈSE N^{O} 5534 (2012)

PRÉSENTÉE LE 9 OCTOBRE 2012

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DES DISPOSITIFS NANOÉLECTRONIQUES
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Suisse
2012

أَلطّرُقُ كَثِيرَةٌ ... الاَ أنَ أَلـهَدَفَ واحِدٌ

The paths are many ... But the goal is one.

Ibn-Rumi 1207 AD

Abstract

Performance improvement by device scaling has been the prevailing method in the semiconductor industry over the past four decades. However, current silicon transistor technology is approaching a fundamental limit where scaling does not improve device performance. As the density of number of devices increases a rise in dynamic and especially static power dissipation is ever more present, making this the biggest issue in microelectronics today. Planar silicon devices are therefore already being replaced by multiple-gate architectures and will be replaced by new channel materials and new switching mechanisms during the next 10 years. A means to decrease the threshold and supply voltage and, therefore minimizing power dissipation, is to employ devices which exhibit a steeper slope than the MOSFET limit of 60 mV/dec at room temperature. The Tunnel FET promises steep turn-on characteristics and low leakage currents as compared to MOSFETs which make it attractive for low-power operation. A great deal of work over the past years has been done to boost device performance of Tunnel FETs by combining ultimate wrap-gate architectures, incorporation of III/V materials and band engineering for hetero-tunnel junctions. The latter is seen as an ideal route towards achieving high drive currents and steep sub-threshold slopes at low supply voltages. This thesis investigates both Si Tunnel FETs and the route towards heterostructure Tunnel FETs, but also the technological challenges to achieve these device structures.
The first part of this work deals with vapor-liquid-solid grown silicon *in-situ* doped n^+-i-p nanowire Tunnel FETs in a lateral geometry, where the influence of the gate dielectric, i.e., SiO_2 or HfO_2, on device performance is investigated along with the study of low-temperature behavior. The devices having the strongest gate coupling due to the high-κ gate oxide HfO_2 are shown to exhibit the best device performance as compared with the SiO_2 gate stack. A vertical process for Si FETs is developed and improved to obtain a fully wrap-gate geometry. It is adaptable to different material systems and is the basis for the ongoing work on InAs-on-Si nanowire Tunnel FETs. Improved performance for these heterostructure devices requires in particular high doping concentrations as well as abrupt doping profiles to achieve high tunnel currents.

Therefore, the second part focuses on the InAs material system and specifically the study of dopant incorporation. Doping is done *in-situ* using different precursors during growth. The InAs nanowires are grown in SiO_2 mask openings on ⟨111⟩ Si substrates in a metal-organic vapor phase epitaxy process. The effect of the dopants and growth parameters on radial and vertical growth rates, wire morphology and resistivity is investigated. A method utilizing the measured Seebeck coefficient of the InAs nanowires to extract doping densities without the need of assuming a mobility value is presented. Two other reference methods where *I-V* characteristics of homo-and heterojunction InAs tunnel diodes are fitted by TCAD simulations confirm this approach. Doping densities ranging from $1{\cdot}10^{17}$ cm^{-3} to $7.1{\cdot}10^{19}$ cm^{-3} were achieved which is comparable to the highest doping concentration reported in bulk InAs.

Furthermore, single vertical pn^+-junctions are fabricated by growing n-type InAs nanowires on p-type InAs substrates, which show high tunnel current densities of 500 kA/cm^2 at 0.3 V reverse bias. In the forward direction, negative differential resistance is obtained below 200 K, which is the characteristic feature of an Esaki diode. **Keywords: Silicon nanowire, Gate-All-Around Tunnel FET, InAs, doping, Tunnel diode, Seebeck coefficient.**

Zusammenfassung

Leistungsverbesserung dank Transistor Skalierung war die bestimmende Methode der Halbleiterindustrie in den letzten 4 Jahrzehnten. Die derzeitige Transistor Technologie nähert sich allerdings einem fundamentalen Limit wobei weitere Skalierung nicht die gewünschte Leistungsverbesserung bringt. Je höher die Dichte der Anzahl an Transistoren wird, desto mehr erhöhen sich die dynamischen und statischen Energieverluste, was dazu führt, dass dieser Energieverlust das grösste Problem in der Mikroelektronik ist. Planare Silizium Transistoren werden deshalb schon heutzutage mit 'multi-gate' Geometrien ersetzt und es ist nur eine Frage der Zeit bei der sie mit neuen Materialien im Transistorkanal und mit neuen Schaltungsmechansimen ersetzt werden. Eine Möglichkeit diesem Energieverlust entgegenzuwirken ist die Schwellen- und Betriebsspannung zu senken indem man Transistoren mit Anschaltkurven, die steiler als der MOSFET Limit von 60 mV/dec sind, einsetzt. Der Tunnel FET verspricht steilere Anschaltkurven und tiefe Leckströme im Vergleich mit einem MOSFET und ist daher gut geeignet für Applikationen wo niedrige Energien eingesetzt werden. In den letzten Jahren wurde viel geleistet im Bereich des Tunnel FET um die Leistung zu verbessern, dies indem man 'wrap-gate' Geometrien, den Einsatz von III-V Materialien und die Bandkanten-Manipulation bei Heterostrukturen verwendete. Letzteres wird als viel versprechend angesehen um höhere An-Ströme sowie steilere Anschaltkurven bei niedrigeren Spannungen zu erzielen. Diese Doktorarbeit erforscht Si Tunnel FETs und den Weg zu Heterostruktur-Tunnel FETs sowie die technischen Anforderungen die erziehlt werden müssen um solche Transistoren zu bauen.
Der erste Teil dieser Arbeit befasst sich mit lateralen n^+-i-p *in-situ* dotierten Si Nanodraht Tunnel FETs, gewachsen mit der vapor-soli-liquid Methode. Der Einfluss von verschiedenen Gate-Oxiden, SiO_2 oder HfO_2, auf die Transistor Leistung sowie die Eigenschaften bei tiefen Temperaturen werden untersucht. Der Transistor mit der stärkeren Gate-Kopplung aufgrund der hohen Dielektrizitätskonstante, nämlich HfO_2, zeigt die besten Ergebnisse. Ein vertikaler Fabrikationsprozess wird entwickelt und verbessert um eine ganzachsige "wrap-gate"Geometrie zu bekommen. Der entwickelte Prozess ist anwendbar auf unterschiedliche Materialsysteme und er ist auch die Basis für den Fabirkationsprozess des InAs-auf-Si Tunnel FETs in unserer Gruppe. Um die InAs-auf-Si Tunnel FETs weiterhin verbessern zu können muss die Dotierungskonzentration im InAs Nanodraht genau kontrolliert werden und gleichzeitig muss man schärfere Dotierungsübergänge erzielen.
Deswegen richtet sich der zweite Teil der Arbeit dem InAs Material System und gezielt der Dotierung. Die Dotierung hier erfolgt mit verschiedenen Ausgangsmaterialien *in-situ* während dem Wachstum. Die InAs Nanodrähte werden auf ⟨111⟩ Si Substraten aus SiO_2 Maskenöffnungen heraus gewachsen durch die metal-organic-vapor-phase-epitaxy Methode. Der Einfluss verschiedener Dotierstoffe sowie Wachstumsparameter auf die Morhphologie, radiale und vertikale Wachstumsrate und den spezifischen elektrischen Widerstand wird untersucht. Eine Methode wird verwendet, die den gemessenen Seebeck Koeffizienten der InAs Nanodrähte benutzt um die Dotierungskonzentration zu bestimmen. Dies ermöglicht eine Bestimmung ohne dass man die Mobilität kennen muss. Zwei weitere Referenzmethoden werden ausserdem benutzt: Die TCAD Simulation von Strom-Spannungs Kennlininen von Homo-und Heterostruktur Tunnel Dioden. Dotierungskonzentrationen im Bereich von $1{\cdot}10^{17}$ cm^{-3} bis $7.1{\cdot}10^{19}$ cm^{-3} werden errreicht wobei die höchste Dotierungskonzentration der höchsten Konzentration im makroskopischen InAs Kristall entspricht.
Es werden ausserdem einzelne pn^+ Übergänge hergestellt aus n-InAs Drähten gewachsen auf

p-InAs Substraten. Diese Dioden weisen sehr hohe Tunnelströme im Bereich von 500 kA/cm^2 bei 0.3 V Rückwärtsrichtung auf. In Vorwärtsrichtung kann ein negativer differentieller Widerstand unter 200 K beobachtet werden, das Kennzeichen für eine Esaki Diode. **Stichwörter: Silizium Nanodraht, Gate-All-Aroung Tunnel FET, InAs, Dotierung, Tunnel Diode, Seebeck Koeffizient.**

Acknowledgements

This thesis marks the end of four years of work in the Nanoelectronics Group at the IBM Research lab in Zurich and my affiliation with the Nanolab at EPFL. The results obtained would not have been possible without the help and support of so many people. I feel grateful that I had the opportunity to work together with smart and talented colleagues.

First, I would like to thank my thesis advisors Dr. Heike Riel and Prof. Adrian Ionescu for providing me with the opportunity to perform this work. I thank Dr. Heike Riel for encouraging me throughout the thesis, her insightful ideas and inspiration were priceless. It was a pleasure working in her group! I am very thankful to Prof. Adrian Ionescu who gave me the freedom and support during my research and I appreciate his kindness and the great working environment he created.

I would like to express my gratitude to the members of the jury who took their time to carefully read through my work and provide me with sound feedback. I thank Prof. Martin Gijs, Laboratory of Microsystems at EPFL, Prof. Anna Fontcuberta i Morral, Laboratory of Semiconductor Materials at EPFL, Prof. Joachim Knoch, head of the Institute of Semiconductor Electronics at RWTH Aachen University and especially Prof. Theresa Mayer, Mayer Group at Penn State University, for making the long trip to Switzerland for the oral examination.

I thank Dr. Walter Riess at IBM Research Zurich, for his ongoing support and inspiration as my former group head and now department head as well as former professional judoka.
In addition, my thanks go out to present and past members of the entire Nanoelectronics Group. Dr. Mikael Björk, from whom I have learned so much and who was a mentor to me throughout my PhD work, thank you for everything.
Dr. Kirsten Moselund, with whom I have worked on the nanowire devices and who taught me valuable measurement skills and processing work, thank you for all your help. It was always fun in and around the lab. Heinz Schmid, who always shared a smile and a laugh, and who was an excellent coach in device processing and a guide in the device work. Dr. Siegfried Karg, thanks for leading me in the right direction many times with fruitful discussions and help. I acknowledge the help from Dr. Emanuel Lörtscher (keep up running!), as well as from Dr. Bernd Gotsmann and Dr. Volker Schmidt. I thank Cedric Bessire, Philipp Mensch (keep on rowing!), Antje Rey, and Giorgio Signorello, it was wonderful to work together on various projects. Good luck with your PhD!
The presence of all people in the group created a great work environment and many discussions contributed to this thesis. Dr. Valentina Troncale, Dr. Pratyush Das Kanungo, Florian

Schwarz, Dr. Peter Nirmalraj, Fabian Menges, Dr. Mattias Borg and Dr. Marius Trouwborst, it was a great pleasure to work with you. Thanks to Dr. Mirja Richter, my great office mate and the person who grew our MBE layers. Thanks for reading through the manuscript.

It would be unthinkable to finish any device batch on time without the technical support of Meinrad Tschudy, Daniele Caimi, Rene Beyeler and Richard Stutz. I often depended on the expertise of Ute Drechsler when it came to processing issues as well as all the fruitful discussions with her and Dr. Dave Webb, who is truly a semiconductor technology veteran. Special thanks to Prof. Andreas Schenk whose TCAD simulations are greatly acknowledged for this work. Furthermore, I would like to thank the team at IBM Yorktown for the TEM images. Also, I would like to thank Luca de Michielis and Livio Lattanzio at Nanolab for their help and insightful discussions. Marie Halm, thank you so much for your help on dealing with everyday things at EPFL. I thank Karin Jaymes for her administrative support.

Outside the lab, I would like to thank the people I studied with, namely Dr. Sebastian Walter, Ivan Tomka, Thomas Merz, Anton Kulik, Milan Calic and Dr. Georg Goetz. It remains in good memory, the laughs we shared, the interesting discussions we had and the nights we spent solving exercises.

The decision on which studies to choose is taken in high school. My chosen path was truly inspired by my dear teacher, Dr. Wolfgang Wiener. I have learned a lot more from him than just the school curriculum provided. I am also grateful to my Physics and Mathematics teacher, Dr. Alfred Dominik, who motivated and inspired me to study natural sciences.

I am fortunate to have great friends, from my early kindergarten friend Mark Erbel to friends in Saudi Arabia, Rayan Kareem and Zurich, Samir Arain and John Bardugone. They made life outside work enjoyable.
Furthermore, I like to thank my parents Wafik and Ingrid for all their love and support during the thesis and who can fully relate to how it is to write one. To my sister Laila and nephew Samy, I am looking forward to teaching Samy all about science as he grows up. They all encouraged me and kept me going strong.
Mary, Tony, Lindsay and Mike, thanks for all the support and understanding concerning my thesis, and thank you for the warmth and kindness you have shown to me.

Finally, Danielle, for whom this work is dedicated and for whom I am thankful for all her love and support. Without you, I would have never made it this far. I love you.

Zurich, October 17th 2012 H. G.

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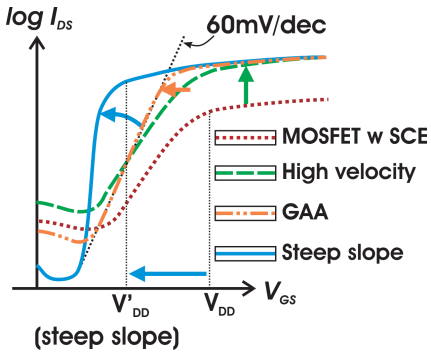
Thesis Overview

Current silicon transistor technology is approaching a fundamental limit where scaling does not lead any more to improved device performance, but rather to increased short channel effects (SCE). Thus, planar silicon devices are expected to be replaced by multiple-gate architectures, new channel materials and new switching mechanisms throughout the next 10 years. A promising new switch candidate combining ultimate wrap-gate architectures and a new switching mechanism based on band-to-band tunneling (BTBT) is the nanowire Tunnel FET. It promises low leakage currents and steep subthreshold slopes lower than the 60 mV/dec limit at room temperature of Si MOSFETs. Thus, there is potential for Tunnel FETs to reduce both the dynamic and passive (leakage) power. Although promising results of Tunnel FETs have been reported, a limiting factor is still the low on-current.

This thesis will discuss bottom-up fabricated nanowire Tunnel FETs, Tunnel diodes and a route towards a vertical heterostructure Tunnel FET based on a Si platform. It starts off by presenting single lateral Si nanowire Tunnel FETs grown by the vapor-liquid-solid (VLS) method. A process for vertical Si FET devices is developed and vertical Si nanowire FETs are presented. The process which is developed is adaptable to different material systems and is the basis for the ongoing work on InAs-on-Si nanowire Tunnel FETs. Improved performance for these heterostructure devices requires in particular the control of doping concentrations in the source and drain as well as abrupt doping profiles to achieve high tunnel currents. A thorough investigation of dopant incorporation in InAs nanowires grown by selective area epitaxy in a metal-oxide-vapor-phase-epitaxy (MOVPE) tool will then be presented. Furthermore, first vertical tunnel diodes based on n-doped InAs nanowires grown on p-InAs substrates are electrically characterized.

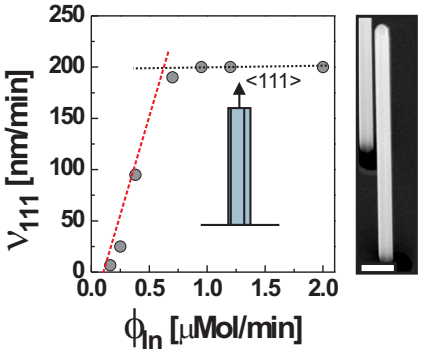
0.1 Outline

Chapter 1: Introduction



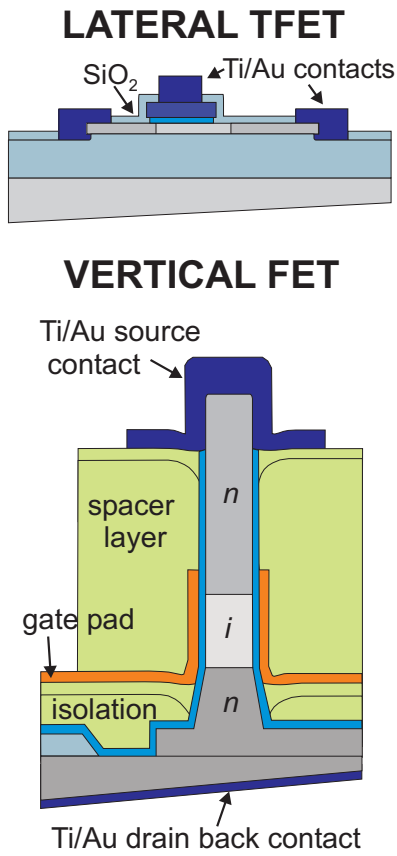
Chapter 1 gives an introduction to MOSFET scaling throughout the past 40 years. It continues by describing the limitations nanoelectronics is facing and why further conventional CMOS scaling is not sufficient any more. The current "power crisis" is described. Different options are then introduced to circumvent the energy problem which arises at ultimately scaled devices. One of these approaches are steep slope devices and in particular, the Tunnel FET. The operation principle of tunnel diodes, an important test structure to study the tunneling junction, is then discussed, followed by the working principle of Tunnel FETs, performance boosters thereof and a short overview on current state-of-the art Tunnel FETs.

Chapter 2: Nanowire Growth and *in-situ* Doping



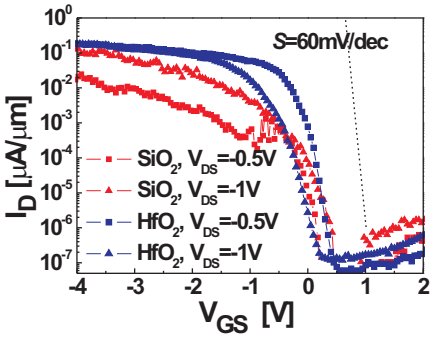
In this chapter the VLS growth of Si nanowires and MOVPE growth of InAs nanowires is described. Both materials are doped *in-situ* during growth and the different growth parameters are discussed. Specifically for InAs, different growth conditions lead to a change in the distribution coefficient altering the incorporation of dopants, as will be shown in chapter 5.

Chapter 3: Device Fabrication



In chapter 3 the fabrication of all devices studied in this thesis is presented. Lateral structures with *in-situ* *p-i-n* and *p-n* doping profiles are used to fabricate diodes and Tunnel FETs. Tunnel FETs with two different gate stacks are fabricated, a gate stack with 20 nm SiO_2 gate dielectric and 5 nm high-κ HfO_2 gate dielectric. A special 'gate-first' process flow is developed for samples with a HfO_2 gate dielectric due to the limited etch selectivity and slow etch rate of HfO_2 in BHF solutions. A full vertical process for Si FETs is also developed. Processing issues which arise during fabrication are discussed and solutions are provided resulting in an improved process. The vertical process is also the basis for the ongoing development of vertical InAs on Si Tunnel FETs in our group and is shown as proof of concept for single vertical FETs. Furthermore, fabrication of vertical InAs Esaki diodes is presented.

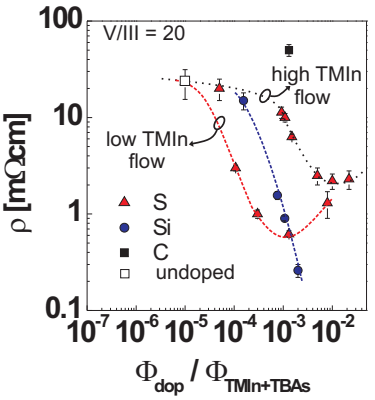
Chapter 4: Characterization of Si-based Devices

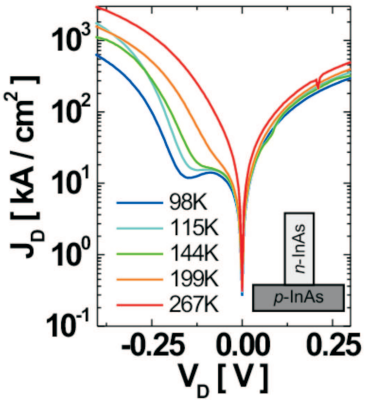


Chapter 4 starts with discussing electrical measurements of *p-i-n* and *p-n* Si nanowire diodes. Electrical characteristics of lateral tunnel FETs are then presented. A high-κ HfO_2 gate stack having stronger gate coupling as compared to SiO_2 leads to improved device performance. The devices have an average slope of $S \approx 120$mV/dec over 4 decades. The on-current is 4× higher for the sample with a HfO_2 gate stack. The presence of a potential barrier limiting the on-current at the p-type side of the tunnel FETs due to the Ti/Au contact is revealed by temperature-dependent measurements. Furthermore,

vertical pMOSFETs are studied electrically. The low on-current seen with all pMOSFETs stems from the small contact length of the top contact or the presence of a thin oxide barrier between the metal and nanowire.

Chapter 5: Doping of InAs Nanowires and Realization of Tunnel Diodes





In-situ doping is an effective method to control doping levels and in particular junction abruptness in nanowire Tunnel FETs. The first part of this chapter studies the effect of various group-IV and group-VI doping species on nanowire morphology, axial and radial growth rates, as well as electrical properties. A method utilizing the measured Seebeck coefficient to extract doping densities without the need of assuming a mobility value is presented. Two other reference methods where *I-V* characteristics of homo-and heterojunction InAs tunnel diodes are fitted by TCAD simulations confirm this approach. Doping densities ranging from $1{\cdot}10^{17}$ cm^{-3} to $7.1{\cdot}10^{19}$ cm^{-3} are achieved, comparable to the highest doping concentration reported in bulk InAs. When using sulphur as a dopant compensation effects occur at very high concentrations. The samples showing compensation exhibit an increase in the Seebeck coefficient by 2.5 compared with bulk. This increase is assumed to stem from charged sulphur complexes in the InAs crystal which lead to an increase in the scattering rate of carriers. In the second part homojunction tunnel diodes are studied electrically revealing negative differential resistance (NDR) behaviour below 200K with a peak current to valley ratio (PCVR) of about 1.4 and current densities in the range of 500 kA/cm^2 at 0.3 V reverse bias at room temperature.

Chapter 6: Conclusion

In the end the experimental results are summarized and discussed. An outlook on the work will be presented.

1 Tunnel FETs for Low-Energy Switching

1.1 Introduction into Scaling in CMOS

Ever since the invention of the point-contact bipolar transistor in 1947 by W. Shockley, J. Bardeen and W. Brattain [SBB47] and the invention of the Si-based bipolar integrated circuit (IC) in 1959 the pace of performance improvement of the semiconductor industry is unprecedented in technology history. The semiconductor industry has shaped the way we deal with information, how we communicate with one another and how we live our everyday lives. From the early Si-based bipolar ICs further refinements of the Si/SiO_2 materials system and technology were achieved and the addition of a silicon gate process led the way to the introduction of field-effect devices, with the metal-oxide-semiconductor field-effect (MOSFET) transistor becoming the most important device. It was reported by Kahng and Atalla in 1960 [KA60] as an outgrowth of the patented FET design and is the foundation of today's semiconductor industry. A distinct characteristic of the evolution of IC technology is that the physical size of the transistor is continuously reduced, thus decreasing cost and increasing performance. This trend was enabled by lithography, the way transistors are fabricated, and which determines the feature size. In 1965 Gordon Moore made his famous formulation [Moo98] that the number of transistors on ICs roughly doubles every two years. The formulation did not just describe the density of transistors that can be achieved, but also the density at which the cost per transistor is the lowest. From then on further innovation such as the use of a polysilicon gate as well as the complementary metal-oxide-semiconductor device (CMOS) by 1968, led to the development of a technology where the gate is self-aligned to the source/drain of the device. Along with the miniaturization of the feature size a significant reduction in power dissipation

and increase of the overall frequency/switching performance of the IC was achieved. This can be seen when looking at the device metrics of a MOSFET, such as drain current in the linear region $I_{D,linear}$, the saturation current $I_{D,sat}$, off-current I_{off}, the switching delay τ and switching energy E [Mei95], [MD00], [MCD01], [TN+98]:

$$I_{D,linear} = \frac{\mu_{eff}\epsilon_{ox}}{t_{ox}} \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \tag{1.1}$$

$$I_{D,sat} = \frac{\mu_{eff}\epsilon_{ox}}{t_{ox}} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{1.2}$$

$$I_{off} \propto 10^{-(V_{th}/S)} \tag{1.3}$$

$$\tau = L_{ch}/v_s \tag{1.4}$$

$$E = 1/2 \times \frac{\epsilon_{ox}}{t_{ox}} (V_{DD} \times L_{ch})^2 \tag{1.5}$$

Here μ_{eff} is the effective mobility, ϵ_{ox} the gate dielectric permitivity, t_{ox} the gate dielectric thickness, W and L the gate width and length respectively, V_{GS} the applied gate bias, V_{th} the threshold voltage, V_{DS} the drain-to-source potential, V_{dd} the supply voltage, L_{ch} the channel length and v_s the saturation velocity.

Specifically the energy E which is stored on the capacitive gate and transferred during a binary switching transition of a MOSFET, is directly proportional to the channel length as well as the switching delay τ (equation 1.5 and 1.4, respectively). In other words, the energy governing a switching event as well as the speed at which the switching takes place is directly proportional to the channel length L_{ch}. The ongoing miniaturization was therefore not only driven by an increased transistor count per chip but also a faster and more efficient device when scaling down the channel length. The rules which were set up for scaling a MOSFET maintaining the electric field in the device and the experimental verification thereof where introduced in 1974 by Dennard at IBM [DGR+74]. The rules are summarized in table 1.1. A dimensionless scaling factor κ is introduced by which both the horizontal and vertical device dimensions are shrunk by the same amount. The applied voltage is also scaled down accordingly while the body doping is increased by κ. This causes the depletion regions within the device to scale in the same way as the physical dimensions. The scaling rules are referred to as constant field scaling because the electric fields within the device are kept constant by scaling the voltage and depletion layer. An increase in electric fields would result in electrons acquiring higher energies and thus, hot electron and dielectric breakdown effects would occur.

These rules don't indicate that there is a fundamental limit to scaling and over the past 4 decades (≈1960s-2000) the energy transfer associated with binary switching was decreased by about 5 orders of magnitude and the number of transistors per chip increased by 9 orders of magnitude!

Table 1.1: Scaling MOSFET devices and IC parameters

Device or Circuit Parameter	Scaling down by
Device Dimension t_{ox}, L_G, W	$1/\kappa$
Electric Field	1
Doping Concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $C=\epsilon A/t$	$1/\kappa$
Delay Time/circuit $\tau=VC/I$	$1/\kappa$
Power Dissipation/circuit $P=VI$	$1/\kappa^2$
Power Density VI/A	1

1.2 Limitations of Scaling

1.2.1 Device and Power Scaling Limits

As scaling has increased transistor density on chips as well as transistor performance, over the past 15 years it has been increasingly difficult to scale the supply voltage V_{DD} and maintain the constant increase of speed.

Short Channel Effects

The limited scalability of the supply voltage V_{DD} is limited by the inverse subthreshold slope S. This is illustrated in Fig.1.1. In Fig.1.1 A a MOSFET is schematically shown with given surface potential ϕ_S [1]. The exponential screening of potential variations in the channel are on the length scale of λ. When scaling down the channel the source-drain distance gets smaller and the depletion zones of the source and drain side overlap. Thus, the overall barrier is reduced and the source-drain potential will have a strong effect on the band bending over a significant portion of the device leaving only a fraction of charge controlled by the gate. The fields of the source and drain can penetrate into the channel lowering and modulating

[1] The surface potential will be more thoroughly introduced in section 1.3

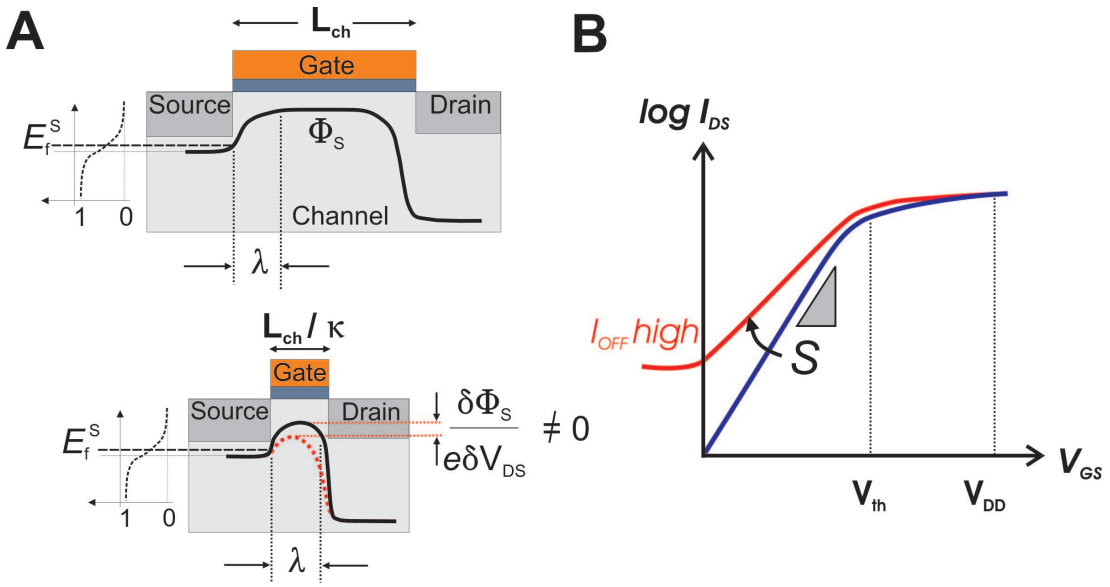


Figure 1.1: Illustration of short-channel effects **(A)** Scaling down the channel length of a MOSFET beyond the limit of $L = 4 \times \lambda$, leads to SCE due to overlapping junctions. **(B)** An increase of I_{off} and decrease of the subtreshold slope S is the outcome of a device operating with SCEs.

the potential barrier between source and drain with the applied drain voltage, referred to as drain-induced barrier lowering (DIBL). This can be seen as the red-dashed line in the lower part of Fig.1.1 A. This effect is called short-channel effect (SCE). The influence of SCE on device characteristics is illustrated in Fig.1.1 B where the transfer characteristics of a MOSFET without (blue curve) and with SCE (red curve) is shown. The threshold voltage V_{th} decreases (V_{th} roll-off) due to DIBL and the inverse subthreshold slope S increases due to diminished gate control over the channel. This leads to an increase of the off-current I_{off}. Additionally, in the output characteristics the current does not saturate any more because $\delta\Phi_S / e\delta V_{DS} \neq 0$. As a consequence the device which has been turned off by lowering V_{GS} below V_{th} can accidentally be turned on by increasing V_{DS}.

Power-Constrained Scaling

The increase of I_{off} as device scaling evolved has had far reaching consequences on the constant field scaling rules by Dennard. Fig.1.2 depicts the trend of scaling V_{DD} and V_{th} down from the 1.4 μm to the 65 nm technology generation. The supply voltage V_{DD} decreased faster than the threshold voltage V_{th} and therefore the gate overdrive, V_{DD} - V_{th}, decreased as well.

A low V_{th} is generally desirable for high on current (see equation 1.2). Therefore, in order to maintain a sufficient gate overdrive, the scaling of V_{DD} has slowed down substantially over the past 15 years. As V_{DD} did not scale with the same factor as the device dimensions the power density, $P = V_{DD} I_{on} / Area$ (Table 1.1) increased.

The switching energy for a a logic operation can be written as [HZB+06]:

$$E_{tot} = E_{dynamic} + E_{leakage} = \frac{1}{2}\alpha C_L V_{DD}^2 + I_{OFF} V_{DD} t_{delay} \tag{1.6}$$

where α is an "activity factor" given by the average number of transitions on a node per clock cycle. C_L is the total load capacitance of a single inverter and t_{delay} is the circuit delay time. Here, I_{off} is the sum of all leakage currents in the MOSFET in the off-state. It is apparent from equation 1.6 that if V_{DD} does not decrease while the device dimensions decrease, the leakage energy dissipation contributes a significant part to the energy balance. Another factor is the increase of I_{OFF} because of leakage through the thinner gate oxide. This in-proportion of scaling resulted in that the leakage power density did not scale with the channel length resulting in a continuous increase as seen in Fig.1.2 B.

The limited scalability of V_{DD} was shown above to increase the total power consumption

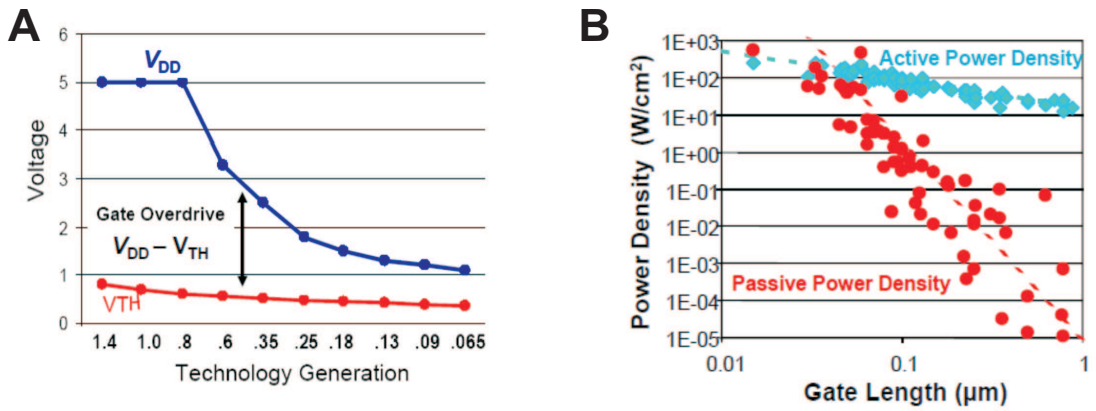


Figure 1.2: **(A)** Threshold voltage and supply voltage scaling as a functuion of technology generation given in μm. **(B)** Increase in passive and active power with decreasing gate length [Pac07].

and degrade performance. The question arises whether scaling down V_{th} to keep a high gate overdrive V_{DD} - V_{th} is possible while controlling SCE in MOSFETs?

The inverse subthreshold slope is defined as the slope of the transfer characteristics from the

off to the on transition. The inverse subthreshold slope S of a MOSFET is given by [TN+98]:

$$S = \frac{\partial V_{GS}}{\partial(\log I_D)} = \underbrace{\frac{\partial V_G}{\partial \Phi_S}}_{m} \underbrace{\frac{\partial \Phi_S}{\partial(\log I_D)}}_{n} = \left(1 + \frac{C_{S,D} + C_B + C_{it}}{C_{ox}}\right) \frac{kT}{q} \ln 10 \tag{1.7}$$

where V_G and Φ_S are the gate voltage and the silicon surface potential respectively, I_D is the drain current, $C_{S,D}$, C_B, C_{it} and C_{ox} are the source/drain capacitance, bulk capacitance, interface traps and the gate oxide capacitance, respectively, k is the Boltzmann constant, T is the temperature and q is the elementary charge. The factor m is called the body factor and refers to the change of surface potential when applying a gate voltage V_G. The body factor can be low as 1 for an ideal MOSFET, meaning that a change in gate voltage induces the same amount of change in the surface potential. As no amplification is present in a MOSFET, m can't be smaller than 1. Although for a standard MOSFET m is always larger than 1, it can be less for new device architectures such as electromechanical FETs and ferroelectric FETs [SD07]. In a MOSFET S is mainly limited by the n term which refers to the injection and conduction mechanism of carriers into the channel. It refers to the change of current as a result of the change in surface potential Φ_S. For an electrostatically well-behaved device ($C_{ox} \gg C_S$ and ideal dielectric interface, i.e. C_{it}=0) S is limited to kT/q ln10 which is 60 mV/dec for a MOSFET at room temperature. If SCE are present, however, the minimum of 60 mV/dec is not reached.

1.2.2 Material Limits

The last section introduced the limits of scaling from a device level perspective. Here, the focus is on the channel material. Si as a channel material bears limits on switching energy, transit time and thermal conductance [Mei95]. An inherent limitation of Si on the performance is, for example, the decrease of the effective electron velocity below 10^7 cm/s leading to an increased delay time when scaling down below the 45 nm node [KA08]. Using a channel material with high mobility increases I_{ON} (equation 1.2), as well as decreases τ and thus can lead to a performance increase. The electron mobility for current silicon n-channels varies from 620 $cm^2V^{-1}s^{-1}$ at low inversion carrier density (N_{inv}<10^{12} cm^{-2}) to 250 $cm^2V^{-1}s^{-1}$ for a higher carrier density of N_{inv}=1.2× 10^{13} cm^{-2}. The hole mobility for current silicon p-channels varies from about 150 $cm^2V^{-1}s^{-1}$ to about 60 $cm^2V^{-1}s^{-1}$. Instead, Ge and III-V semiconductors posses higher bulk and electron mobilities, respectively. One strategy is therefore to replace

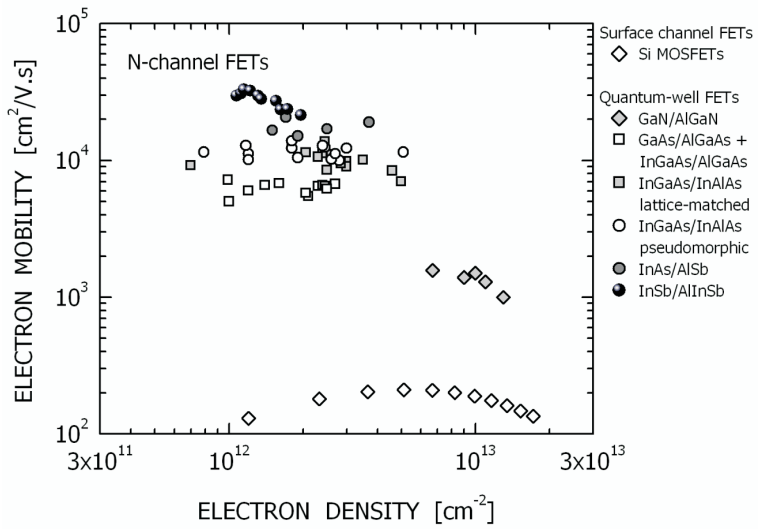


Figure 1.3: Electron mobility vs. sheet electron density in various n-channel Quantum-well FETs in comparison to Si MOSFETs. Figure taken from [CDM05].

silicon channels by other semiconductors, such as SiGe or Ge for p-type channels and III-V materials such as InGaAs, InAs (with an electron mobility of 33000 $cm^2V^{-1}s^{-1}$) or InSb with an electron mobility of 80000 $cm^2V^{-1}s^{-1}$ for n-type channels. Ge has a high electron mobility of 3900 $cm^2V^{-1}s^{-1}$ which is 2.7× higher than the comparable bulk mobility of Si. However, due to a high interface state density D_{it} close to the conduction band, the mobility values for Ge and III-V materials are reduced in practice. The higher field effect mobility of Ge for p-channels and III-V's for n-channels can lead to very high injection velocities which provide both higher on-currents, I_{on}, and lower gate capacitance at constant I_{on}. Fig.1.3 [CDM05] shows the electron mobility vs. sheet electron density in various III-V n-channel Quantum-well FETs compared to that of a Si MOSFET. The III-V FETs exhibit around a hundred times larger electron mobility than Si. This should enable III-V channel based FETs to pertain high enough mobilities in scaled devices. However, many challenges have to be overcome to achieve this performance gain in scalable and integrated FETs. To achieve high complimentary MOS performance, co-integration of different materials (i.e. III-V and Ge) on silicon is necessary. Even though III-V's and Ge have this attractive advantage as shown above, there are still significant technological issues such as defect reduction, interface chemistry, metal contact resistivity, and process integration, which have to be solved before III-V can replace Si as a channel material.

1.3 Device Scaling Options and Advantages of Nanowires

1.3.1 Critical Channel Thickness

The previous sections discussed the limits of scaling at the material and device level. As the gate length is reduced, ideally the gate dielectric thickness has to be scaled correspondingly to control the short-channel effects by increasing the inversion charge and the on-current (see Table 1.1). To alleviate these short channel effects increased channel doping and halo implant has been proposed [BFNS80]. This, however, causes the electron mobility to decrease and the junction capacitance to increase. Additionally, at small length scales dopant fluctuation increases threshold voltage variation [MMR05]. As scaling proceeds, new solutions to reduce parasitic capacitances have been proposed, for example: the partially-depleted (PD) Silicon-On-Insulator (SOI) and the fully-depleted (FD) SOI technology. In a fully depleted channel, the gate control is significantly enhanced due to the thin Si body. Additionally, the almost undoped Si channel minimizes dopant fluctuations which would otherwise lead to threshold voltage variation. SOI-based MOSFETs use a thin Si body to trade off low parasitic resistance for a better control of SCE. It has been experimentally shown that FD SOI MOSFETs exhibit less threshold voltage variation and less DIBL effects than bulk MOSFETs [HMK$^+$10]. All approaches above still don't guarantee that at nanoscale dimensions the channel conductance is predominantly controlled by the gate electrode, and not by the drain which depends strongly on the gate length. SOI and FD SOI devices also achieve better electrostatic gate coupling compared to MOSFETs. Another alternative to achieve better electrostatic coupling is to improve the gate-channel geometry by using multi-gate devices such as e.g.: the planar double gate [HLK$^+$00], finFET [HLK$^+$99], Π-Gate (Triple Gate) [DBD$^+$03], Ω-Gate [YCC$^+$02] and a gate-all-around (GAA) nanowire structure [CGRR$^+$90], all being fabricated with either bulk or SOI technology. Fig.1.4 depicts schematics of several device cross sections, viewed in the direction of the current flow: a planar SOI FET, a double-gate finFET, a tri-gate FET and a Gate-All-Around (GAA) Nanowire FET. To sustain electrostatic integrity the Si channel thickness, t, perpendicular to the channel length has to be below a critical thickness t_c when scaling the gate length. For planar SOI MOSFET channels the critical thickness $t_c \approx L_G/3$ [You89], for a double-gate FinFET $t_c \approx 2/3L_G$, for a Tri-Gate and Ω-Gate $t_c \approx L_G$ and for a GAA channel $t_c \approx 2\cdot L_G$ [YLC$^+$04]. Thus, for the same gate length the criterion to sustain electrostatic integrity over the channel is therefore less strict for GAA structures when it comes to scaling the channel thickness. To describe the electrostatics governing the operation in

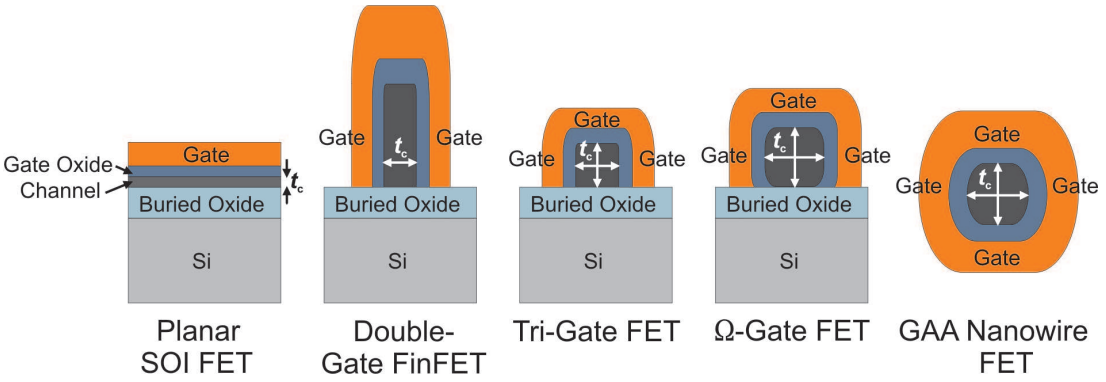


Figure 1.4: Schematics of device cross sections viewed in the direction of the current flow. From left to right: a sing SOI FET, a double-gate finFET, a triple-gate FET, an Ω-Gate FET and a Gate-All-Around (GAA) Nanowire FET. The critical channel thickness t needed to sustain electrostatical integrity as a function of gate length L_G is $t \approx L_G/3$ for planar SOI FETs and $t \leq 2 \cdot L_G$ for GAA Nanowire FETs.

devices, the Poisson equation has to be solved to calculate the electrostatic potential Φ in the channel. This potential governs the injection of carriers from source to drain. The general form of the Poisson equation for ultra-thinbody devices in a single or multi-gate configuration is given by [You89]:

$$\frac{d^2\Phi(x,y)}{dx^2} + \frac{d^2\Phi_S(x,y)}{dy^2} = \frac{q(\rho \pm N)}{\epsilon_{SC}} \tag{1.8}$$

where ρ is the mobile carrier density and N is the constant dopant density in the channel stemming from either donors ("+") or acceptors ("-"). ϵ_{SC} is the dielectric constant of the semiconductor and q the elementary charge. An approximation to solve equation 1.8 is the parabolic Ansatz:

$$\Phi(x,y) = c_0(y) + c_1(y)x + c_2(y)x^2 \tag{1.9}$$

where x and y are the directions perpendicular and along the current direction in the channel, respectively. Depending on the channel geometry the variables can be transformed, for example in cylindrical coordinates when dealing with a nanowire channel structure. As all the information for scaling the gate oxide thickness and channel thickness is contained along the dimension directly at the channel-gate dielectric interface, it is sufficient to solve the Poisson equation along this direction in 1D. Thus, the 1D potential along the channel axis can be written in the same form by neglecting the perpendicular variable which then simplifies to

$\Phi(x=0,y)$=$\Phi_S(y)$. Φ_S refers to the potential at the channel-dielectric interface, termed surface potential. The Ansatz can then be inserted into equation 1.8 with the characteristic boundary conditions of the channel geometry (as single/double/tri gate or gate-all-around). The 1D Poisson equation then simplifies to [STT+93], [You89], [KBR+08]:

$$\frac{d^2\Phi_S(y)}{dy^2} - \frac{\Phi_S(y)-\Phi_G-\Phi_{bi}}{\lambda^2} = \frac{q(\rho \pm N)}{\epsilon_{SC}} \tag{1.10}$$

where Φ_G, Φ_{bi} are the gate potential and built-in potential, respectively. The solution of the 1D Poisson equation 1.10 is of the form:

$$\Phi_S \propto \exp(-\frac{y}{\lambda}) \tag{1.11}$$

[You89] where λ is the screening length which was introduced in section 1.2.1 and which represents the characteristic length scale for channel potential variation. It is a factor which depends on the device geometry as will be shown in the following. For a geometry which utilizes a single gate (SG) [You89], a double gate (DG) [STT+93] or a gate-all-around (GAA) [AP97] the screening length λ is, respectively:

$$\lambda_{SG} = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} t_{ox}} \tag{1.12}$$

$$\lambda_{DG} = \sqrt{\frac{\epsilon_{Si}}{2\epsilon_{ox}} t_{Si} t_{ox}} \tag{1.13}$$

$$\lambda_{GAA} = \sqrt{\frac{2\epsilon_{Si} t_{Si}^2 \ln\left(1+\frac{2t_{ox}}{t_{Si}}\right) + \epsilon_{ox} t_{Si}^2}{16\epsilon_{ox}}} \tag{1.14}$$

where t_{Si}, ϵ_{Si}, t_{ox} and ϵ_{ox} are the physical thickness and the permittivity of Si and the dielectric, respectively. The screening length allows to calculate the minimum gate length where electrostatic integrity is still given. In order to avoid SCE the gate length $L_G \ll \lambda$ [KBR+08]. In this case the gate voltage controls the injection of carriers into the channel one-to-one. Thus, short-channel effects are reduced when the natural length of a device is much smaller than the gate length. For GAA structures such as nanowires with a similar thickness to SG and DG SOI MOSFETs, the screening length is smaller which results in an inverse subthreshold slopes closer to the thermal limit (60 mV/dec) and smaller DIBL at a given gate length. This shows that nanowires, having the GAA geometry, are attractive for further scaling down CMOS.

The advantage of GAA structures is also depicted in Fig.1.5 where the inverse subthreshold slope at V_{DS}=0.1V is plotted as a function of gate length for a double-, triple-, quadruple-/GAA and π -gate (i.e. FinFET) MOSFET. The device width and Si body thickness are kept constant at $W = t_{Si}$=50 nm as well as the oxide thickness t_{ox}=3 nm. It can clearly be seen that better electrostatic control leads to lower inverse subthreshold values at scaled gate lengths.

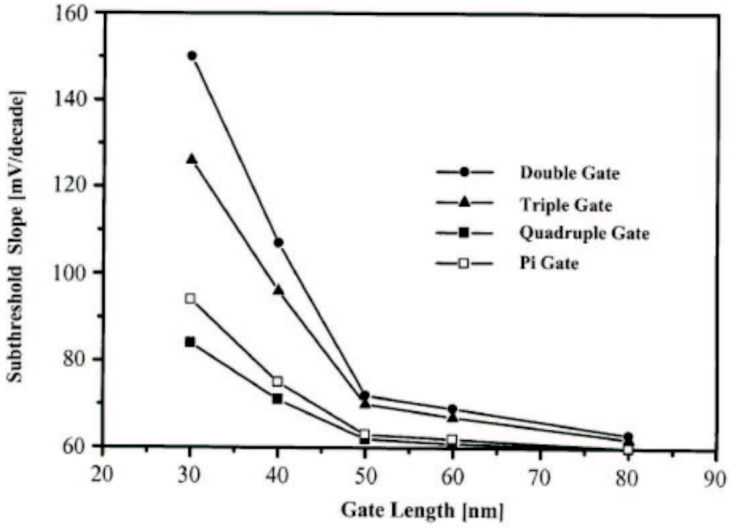


Figure 1.5: Simulated inverse subthreshold slope in double-, triple-, quadruple-/GAA and π -gate MOSFETs as a function of gate length. $W = t_{si}$ = 50 nm, t_{ox} = 3 nm, V_{DS} = 0.1V,[Col04].

1.3.2 Steep Slope Devices

All the approaches to overcome SCE presented so far utilized the same device mechanism, the MOSFET. Fig. 1.6 illustrates these improvements on the MOSFET transfer characteristics. The on-current I_{DS} is shown as a function of gate-source voltage V_{GS} with V_{DD} being the supply voltage. The red dotted curve represents a Si MOSFET device exhibiting short channel effects,

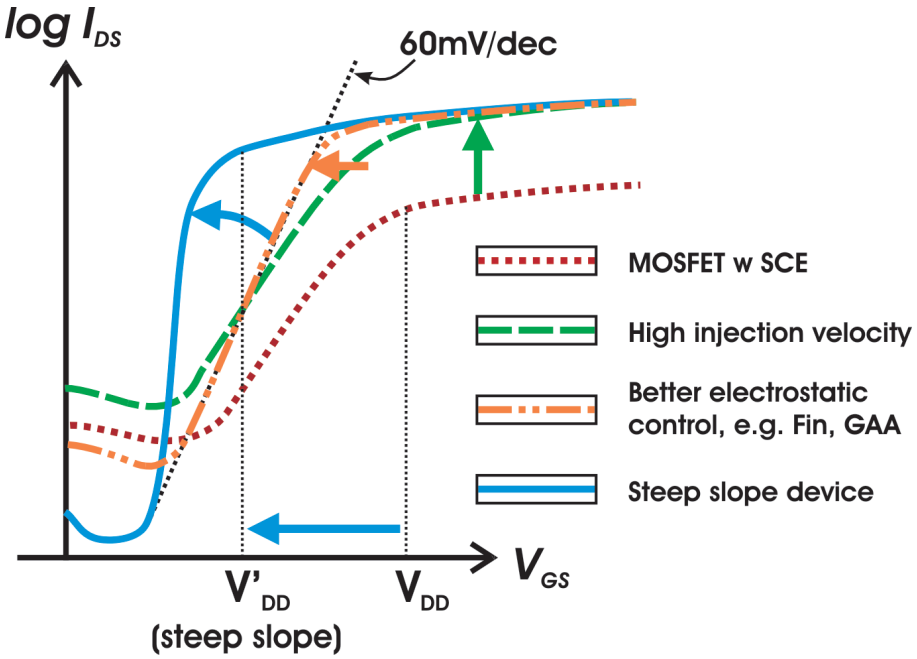


Figure 1.6: Different strategies to enhance performance while further scaling device dimensions. The on-current I_{DS} is shown schematically as a function of gate-source voltage V_{GS} with V_{DD} being the supply voltage. The red dotted curve represents the CMOS limit in a short channel device with degraded substhreshold slope S>60 mV/dec. A device having a channel with a high electron injection velocity is depicted in the green dashed curve. Better electrostatic control by a multi-gated channel increases electrostatic integrity, and thus, restores the thermal limit of 60 mV/dec of the inverse subthreshold slope, which can be seen as the orange dashed-dotted curve. By improving the I_{on}/I_{off} ratio with a steep slope device V_{DD} can be reduced which is shown as the solid blue curve.

with degraded substhreshold slope S (S>60 mV/dec). The following improvements which are schematically shown exclude any defects, interface traps and charges which could further degrade device performance. Replacing the channel with a material having a high electron injection velocity leads to higher on-currents, but not necessarily better inverse subthreshold slopes. This is depicted in Fig.1.6 as the green dashed curve. As explained earlier better electrostatic control by a multi-gated channel restores electrostatic integrity, and thus, restores the thermal limit of 60 mV/dec of the inverse subthreshold slope (see equation 5.5), seen as

the orange dashed-dotted curve in Fig.1.6.

The limited scalability of V_{DD} and the increase in leakage currents have led to a power problem as scaling continues: the power density did not scale with the device dimensions because the leakage power has increased due to rising off-currents I_{off} when scaling down stemming from either subthreshold leakage or oxide leakage. To reduce I_{off} a high-κ gate dielectric with increased thickness t_{ox} can be utilized. However, to reduce the dynamic energy, V_{DD} has to be reduced which means that I_{off} increases at constant S and consequently the leakage energy. This is governed by the limited value of the inverse subthreshold slope which is 60 mV/dec at room temperature. This interplay of leakage and dynamic energy is depicted in Fig.1.7 where the total energy is broken down into leakage and dynamic energy as a function of supply voltage V_{DD}: as the supply voltage is is reduced the leakage energy increases leading to an increase in total energy. A device where the inverse subthreshold slope is not limited to

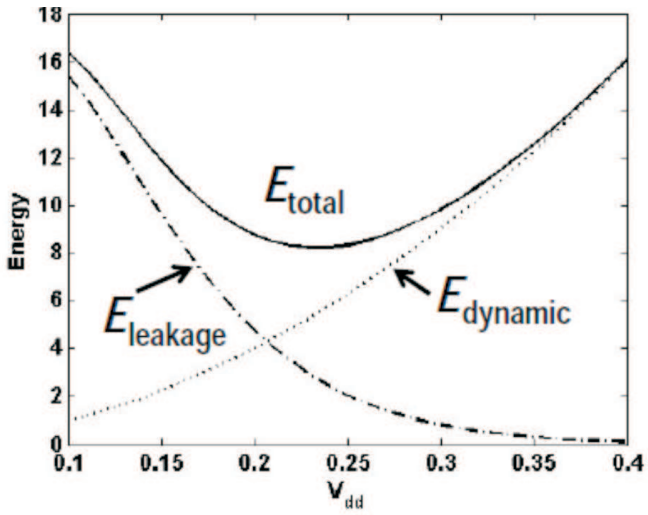


Figure 1.7: Total energy, the sum of dynamic and leakage energy, as a function of V_{DD} showing that while scaling down V_{DD} the leakage power increases and dominates the total energy.

60 mV/dec is needed as a steeper slope allows a significant reduction of the supply voltage V_{DD}. This is shown in Fig.1.6 as the solid blue curve and shift of V_{th} to lower voltages. As already mentioned above, novel devices which have a small swing can be categorized in two sections: those which reduce the body factor m in the inverse subthreshold slope (equation 5.5) and those which lower the n-factor to less than the thermal limit $kT/q\ln 10$. Devices which can lower the body factor are nanoelectromechanical relays [JYK+08], or FETs with a positive feedback gate material such as a ferroelectric material [SD07]. Examples for devices which lower the n-factor by changing the injection mechanism into the channel are devices

based on avalanche breakdown such as the impact ionization MOS (iMOS) [GGP05] or band-to-band tunneling (BTBT) mechanism [RA95]. The iMOS concept is based on a reduction of the inverse subthreshold slope by an amplification of the on-current by avalanche effect. It consists of a gated p-i-n structure where the gate is placed over a part of the intrinsic region either close to the p-or n-segment and operates in reverse bias. At low V_{GS} bias the device is off and with increasing V_{GS} an higher fraction of the source-drain voltage V_{DS} falls across the intrinsic region enhancing both lateral and transverse electric fields. At a certain V_{GS} avalanche breakdown takes place leading to very small slopes down to 5 mV/dec [GGP05]. A drawback for iMOS devices is the limited scalability of the ungated and gated region of the intrinsic segment as well as the high V_{DS} bias needed (≈5V in Si) to reach the breakdown regime. The BTBT mechanism, on the other hand, allows to scale down the supply voltage depending on the material system employed and can reach an inverse subthreshold slopes beyond 60 mV/dec while maintaining low off-currents. Devices where the injection mechanism is based on BTBT have therefore gained lots of attention over the past years and are a promising path to explore the possibilities after CMOS reaches the limit of further down scaling.
In the following section the BTBT mechanism will be described on the basis of the Esaki tunneling diode. The working principle of a three terminal tunneling device, the Tunnel FET, will be then introduced and device parameters explained. Performance boosters will be explained and current state-of-the-art device will be discussed.

1.4 From Tunnel Diodes to Tunnel FETs

In tunnel devices as considered here the charge carriers are injected into the channel via band-to-band-tunneling (BTBT) and consequently, the inverse subthreshold slope S is not limited to the thermal room temperature value of 60 mV/dec [KBR+08]. Therefore, these devices promise to reduce the operating voltage V_{DD} as discussed before and shown in Fig. 1.6. The following section describes principles and operation of an Esaki tunnel diode and what can be done to improve tunneling currents. The properties governing the tunneling junction of an Esaki diode such as tunneling currents, junction quality and influence of doping and material systems thereof are important aspects which have to be taken into account when fabricating Tunnel FETs. An Esaki tunnel diode is therefore a perfect test structure for a Tunnel FET to study the properties of the tunneling junction. The next section introduces the Tunnel FET, its operation principle and device parameters as well as characteristic behavior

of operation compared with a MOSFET. It gives an overview on performance boosters and current state-of-the-art Tunnel FET devices which have been demonstrated.

1.4.1 Esaki Tunnel Diode

The heart of a Tunnel FET is the tunnel junction where carriers are injected into the channel via BTBT through a barrier which is varied by a gate. As mentioned above an Esaki diode is the optimal test structure to study this barrier and facilitate to conclude what material systems lead to the optimal Tunnel FET device. Before turning to the actual Tunnel FET device the operation principle of a tunnel diode is explained. The tunnel diode which first described BTBT was introduced by Leo Esaki in 1959 [EM60]. It consisted of a narrow and degenerate *p-n* junction in Germanium. The working principle of such a diode is shown in Fig.1.8. There are four components of current contributing to the total current, namely the tunnel, valley, excess and diffusion current.

Forward Tunnel Current

At zero bias the Fermi levels are energetically aligned and no current is flowing (Fig.1.8A). As the voltage is increased, electrons at first tunnel through the very narrow p–n junction barrier because filled electron states in the conduction band on the n-side become aligned with empty valence band hole states on the p-side of the p-n junction. This is depicted in Fig.1.8B where the tunnel current is shown as the blue arrow. The according current-voltage characteristics are shown at the bottom right. The tunnel current is given by the transmission probability integrated over all available states [Kar62]:

$$I_T = const1. \int_0^{E_1+E_2-qV} \frac{qV}{4kT} \sqrt{E\left(E_1+E_2-qV-E\right)}\,\mathrm{d}E = const2. \times \frac{V_1}{T}(E_1+E_2-eV_1)^2 \quad (1.15)$$

where E_1 and E_2 are the energy differences from the Fermi level to the conduction band on the n-type side and the Fermi level to the valence band on the p-type side, respectively. V_1 is the applied voltage which is also depicted in Fig.1.8B.

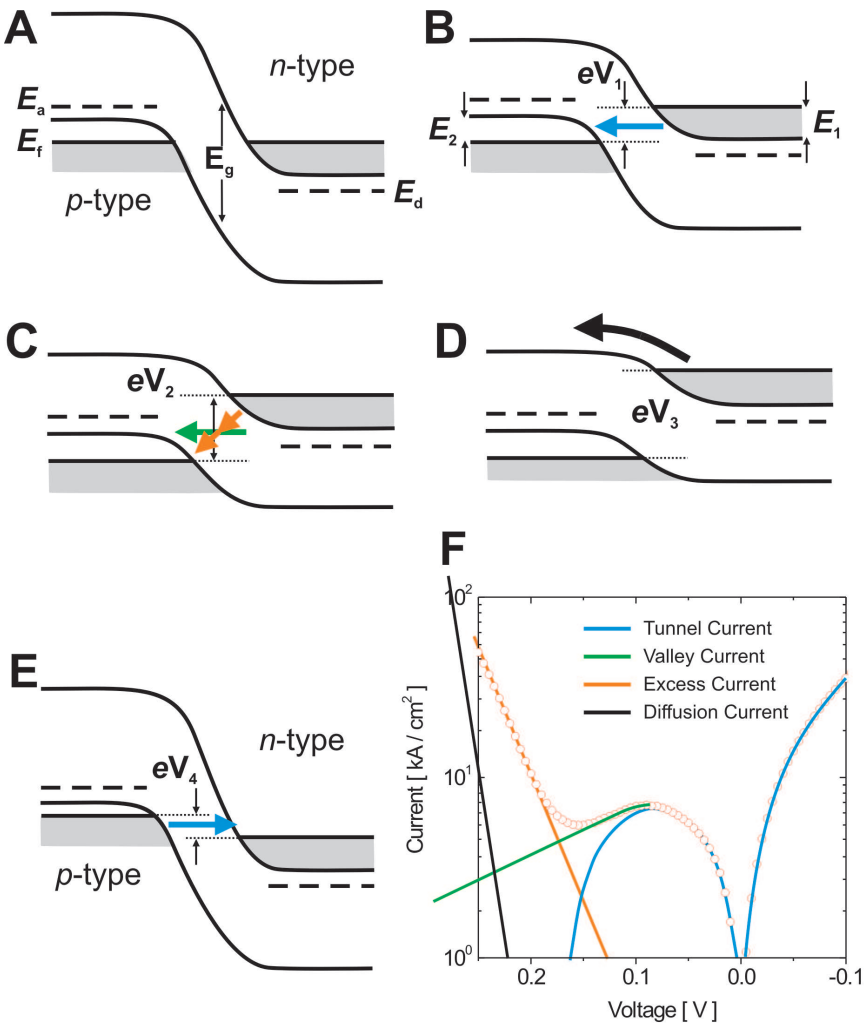


Figure 1.8: Band edge diagram and current-voltage characterisitcs **(F)** of an Esaki diode. **(A)** At zero bias no current flows because both Fermi levels are energetically aligned. **(B)** In forward bias electrons at first tunnel through the very narrow p–n junction barrier due to the alignment of filled electron states in the conduction band on the n-side with empty valence band hole states on the p-side of the p-n junction. The corresponding tunnel current is shown in blue at the bottom right part. **(C)** Valley current due to tunneling between band tail states (green arrow) and interband tunneling excess current (orange arrow) sets in, leading first to a decrease in current at increasing bias voltage, and then to an increase again. This is depicted in the bottom right as the green and orange line. **(D)** At high bias voltage diffusion current dominates and the tunnel diode acts as a normal pn-diode. **(E)** In reverse bias filled hole states in the valence band on the p-side become aligned with empty conduction band electron states on the p-side of the p-n junction. Through this holes start to tunnel through the bandgap leading to a high tunnel current as can be seen in the current-voltage characteristics.

Valley Current

As voltage increases further filled and empty states on the p-and n-side become more misaligned and the current drops as indicated in the bottom right of Fig.1.8F. This is called negative differential resistance (NDR) because current decreases with increasing voltage. In this regime the valley current sets in which is due to tunneling between band tail states [Kan61]. Since the band edges are never sharp in the junction region of degenerate semiconductors the density of states decays exponentially at the p-n junction into the forbidden energy gap. From these states electrons can tunnel into the band states without loosing their energy. This band tails excess current, called valley current, is shown as the green arrow in Fig.1.8C and as the green line in the current-voltage characteristic. The signature of a good quality tunnel junction is a high NDR value because it directly indicates a low trap density in the bandgap. Another signature of a high quality junction is a high peak-to-valley current ratio (PVCR).

Excess Current

A more pronounced mechanism than band tails excess current is interband tunneling excess current which occurs when electrons dissipate their energy such that tunneling can take place. Trap and defect states can form within the bandgap of the p-n junction and can arise due to imperfections in the crystal. Since these states are spread over the entire bandgap electrons can tunnel via bandgap states, loosing their excess energy to neighbouring impurity atoms. The orange arrows in Fig.1.8C and the orange line correspond to this mechanism.

Diffusion Current

When the voltage exceeds a certain value the normal diffusion (or thermal) current will dominate as in the case of the usual p-n diode. This is characterized by lowering the potential barrier of the intrinsic electric field in the junction. Electrons now start to diffuse from the n side to the p side and vice versa for holes as indicated in Fig.1.8D. This leads to a steeper incline in current in comparison to the interband tunneling excess current as seen in the black line at the bottom right in Fig.1.8. The current density for drift and diffusion is:

$$J_{drift,diff} = J_{n,p}(drift) + J_{n,p}(diffusion) \tag{1.16}$$

$$= J_S\left(\exp\left(\frac{eV}{\eta k_B T}\right) - 1\right) \tag{1.17}$$

$$J_S = \frac{k_B T \mu_p p_{n0}}{L_p} + \frac{k_B T \mu_n n_{p0}}{L_n} \tag{1.18}$$

where J_S is the saturation current density, μ_p and μ_n the hole and electron mobility, respectively, p_{n0} and n_{p0} the equilibrium densities of holes on the n side and of electrons on the p side, respectively and L_p and L_n are the diffusion lengths of holes and electrons, respectively. In highly doped p-n junctions the recombination and generation of carriers in the depletion region is not negligible. For the total current in the diffusion regime the recombination and generation current has to be considered. This leads to a reduction in the total current density at an applied bias voltage V and can be generalized as follows:

$$J_{tot} \approx \exp(\frac{eV}{\eta k_B T}) \tag{1.19}$$

Here, η is the ideality factor which equals 1 for an ideal diode. If, however, recombination is dominant, the ideality factor is higher than 1. At high forward biases series resistances R_S can lead to a deviation of the ideal diode current and its reduction by a factor of $\exp(-eIR_S/k_B T)$.

Reverse Tunnel Current

The reverse tunnel current is the operation region of a Tunnel FET as will be shown in the next section. As the tunnel diode is slightly reverse biased the Fermi level in the p-region reaches above the Fermi level in the n-region, opening a tunnel path through the bandgap.

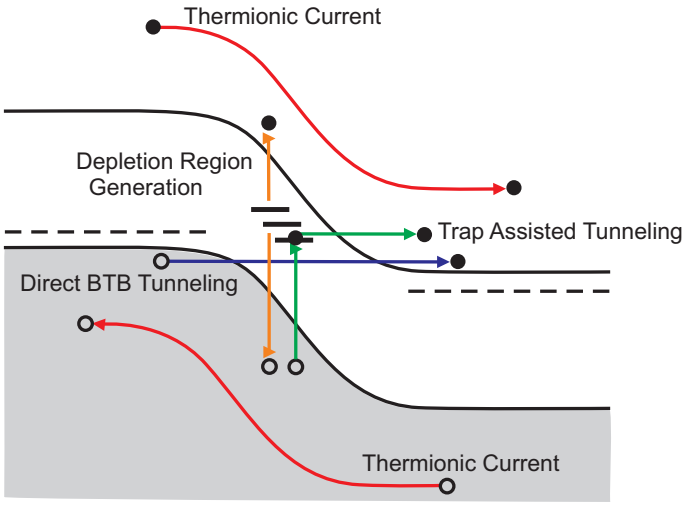


Figure 1.9: Different types of current in a reverse biased pn-junction. Along with thermionic current and direct band-to-band-tunneling two leakage components exist: depletion region generation and trap assisted tunneling. The leakage components degrade device performance of Tunnel FETs.

Thus, holes are injected through the bandgap to the n side. The general equation for the tunnel current (see equation 1.15) is valid again. As in forward bias there are several other mechanisms contributing to the total current. The different types of currents are shown in Fig.1.9 and are important for device performance in a Tunnel FET. Alongside BTBT current, shown in blue, is thermionic emission as depicted in red. The two main leakage currents which can degrade device performance are shown in orange and green. The first (in orange) is a Shockley-Reed-Hall (SRH) generation current where electrons are thermally excited from the valence band to traps within the bandgap and then excited again from the traps to the conduction band. In the second trap assisted process the electron is still thermally excited from the valence band to a trap, but then tunnels out as shown by the green arrows. If traps are a dominant feature within the bandgap the two mechanisms can dominate the total current in reverse bias. Consequently, the energy filtering (which will be introduced in the next section) does not work any more which leads to that lower subtreshold values than 60 mV/dec can not be reached limiting the performance in Tunnel FETs.

In summary, the different types of currents in an Esaki diode are a signature for the junction quality in terms of defects and traps. A high tunnel current is Easki diodes is a prerequisite to achieve high on-currents in Tunnel FETs. All these properties can be studied with an Esaki diode to gain insight on performance factors in Tunnel FETs utilizing the same material system.

1.4.2 Working Principle of the Tunnel FET

Tunnel FETs are gated p-i-n diodes or, less common, p-n junctions. The gate runs along the entire intrinsic region in the case of a p-i-n structure. The gated structure is shown in Fig.1.10A together with the band diagram in the off state. It is an p-type device with the n^+ doped part being the source and the p part the drain. At negative V_{DS} and zero gate voltage current is suppressed by the barrier at the source, channel and drain regions. This results in very low off-state leakage currents. If a negative gate voltage is applied, such that the valence band edge in the channel is pushed above the conduction band edge in source, holes are injected into the channel via BTBT and constitute a drain current I_d as in the case of an Esaki diode (blue arrow in Fig.1.10B). During the BTBT process the energy gaps of the n^+-doped and the

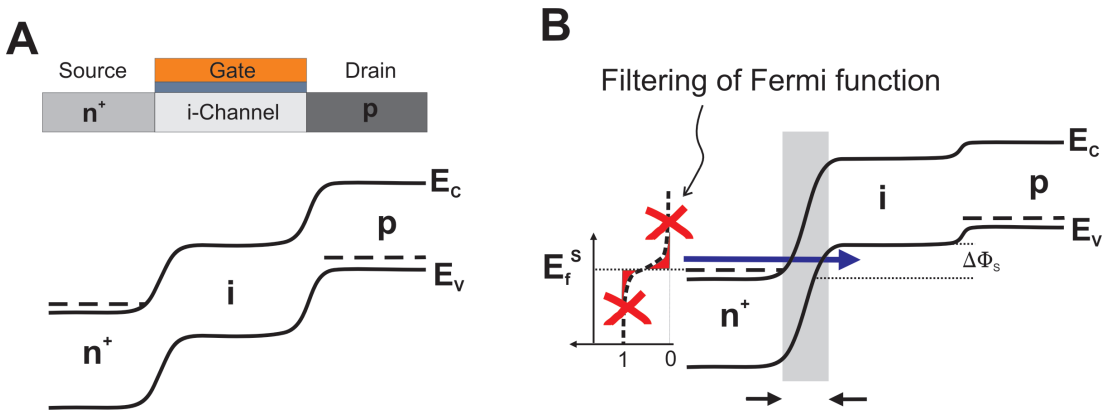


Figure 1.10: Working principle of a Tunnel FET. **(A)**: Gated n^+-i-p structure shown with according band edge diagram. In reverse bias and at zero gate voltage no current flows. **(B)** At negative gate voltage the valence band edge in the channel is pushed above the conduction band edge in source and holes are injected into the channel via BTBT constituting to a drain current I_d. Since only carriers within a small energetic window $\Delta\Phi_S$ contribute to the tunnel current, the device acts as if "cooled down". Higher energetic carriers are "filtered" out from the Fermi function.

gated region of a Tunnel FET act as energy filters, and thus high energetic carriers in the Fermi distribution are suppressed in the current flow. This is depicted by the small energetic window $\Delta\Phi_S$ through which only carriers can tunnel through. By eliminating the high energetic tail of the Fermi distribution, the electronic system gets effectively "cooled down", i.e. the entire system acts like a conventional MOSFET at a lower temperature. This is the reason why in principle, BTBT current can achieve S values smaller than 60 mV/dec. The three terminal Tunnel FET device was first proposed by Baba in 1992 [Bab92] which consisted of an MBE grown n^+-i-p^+ GaAs layer and an insulating AlGaAs gate. The drain part constituting the

p-part was highly degenerate to form a tunnel junction at the i-p junction when a gate bias is applied. By using a GaAs/AlGaAs heterostructure a two-dimensional electron gas (2DEG) channel is formed under the gate close to the surface. It was therefore called a surface tunnel transistor. As these first transistors relied on a 2DEG under the gate the source-gate and drain-gate leakage was high.

To describe the BTBT current and get an overview on device parameters which influence the performance, the tunneling probability at the junction has to be considered. The BTBT current is proportional to the tunneling probability which can be approximated by the Wenzel-Kramer-Brillouin method [AKB+08]:

$$I_{tunnel} = \frac{2e}{h} T_{WKB} k_B T \ln \left(\frac{\exp\left(\frac{\Delta\Phi_S - E_f^S}{k_B T}\right) + 1}{\exp\left(-\frac{\Delta\Phi_S - E_f^S}{k_B T}\right) + 1} \right) \tag{1.20}$$

where E_f^S is the source-Fermi level and T_{WKB} the tunnel probability which is given by [AKB+08]:

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^\star} E_g^{3/2}}{3\hbar(E_g + \Delta\Phi_S} \right) \tag{1.21}$$

In this equation also the screening length or spatial extent λ appears, which was introduced in the previous chapter for a MOSFET device. $m^\star$ is the effective electron mass and E_g the bandgap. Although the above description is valid for a semiconductor with direct bandgap, the same dependencies pertain for λ, $m^\star$ and E_g in a semiconductor with indirect bandgap. One of the challenges in Tunnel FETs is to achieve high enough on-currents. Because only a limited number of states within the energetic window constitute to the tunneling, the current of a Tunnel FET is generally lower than that of a MOSFET. In order to still realize high on-currents the BTBT barrier must be as transparent as possible, i.e. T_{WKB} should be close to unity in the device's on-state. It is obvious that this can be achieved if the spatial extent, i.e. λ, of the transition at the source-channel interface is as small as possible (see Fig. 1.10B). This is also derived from equation 1.21 where the tunnel probability (and thus the tunnel current) is large when the screening length λ is small. As seen in the previous chapter a gate-all-around (GAA) geometry together with high-κ gate dielectrics leads to improved electrostatics and a small screening length. The gate oxide in a Tunnel FET can be scaled down as much as

possible to obtain a higher tunnel probability. Simulations have shown that a decrease in gate oxide thickness decreases the inverse subthreshold slope below 60 mV/dec when all other parameters are kept the same [AKB+08]. Simulations utilizing a high-κ gate dielectric and a double gate showed improved I_{on}, I_{off} and an improvement in the average inverse subthreshold slope S [BI07].

To achieve optimum energy filtering in the source the Fermi energy E_f^S has to be slightly above the conduction band edge in case of an n-doped source contact (or below the valence band in a p-doped source contact). If the Fermi energy in the source is too large, the band gap does not effectively cut off the low (for a p-source the high) energy portion of the source Fermi distribution [AKB+08] and S will not be smaller than 60 mV/dec. Tunnel FETs are usually ambipolar which can be inhibited by an asymmetric doping profile of source and drain. Otherwise the device is always on for both positive and negative gate voltages. A tight control of source and drain doping is therefore necessary. Another way to hinder ambipolarity is to underlap the drain region with the gate. Depending on the operation mode, the drain p-part of the device has to exhibit lower doping than the source n-part or vice versa. This enhances BTBT at the source and suppresses BTBT at the drain in the off state. The energy "filtering" in a Tunnel FET can lead to inverse subthreshold slopes S below 60 mV/dec, but unlike in a MOSFET the S value is not constant in the transition region. This stems from the dependence of conduction and valence band bending on the gate voltage at the tunnel junction and thus, the S value will differ at each gate voltage. The definition of the S value is therefore important. A common way to define the S value is to give an average slope (across the entire transition region) and a point slope which is defined at a certain gate voltage.

A look at the effective electron mass m^* and bandgap E_g in equation 1.21 shows that by choosing a source or channel material at the tunnel junction which has a small bandgap and small effective electron mass the tunnel probability increases and thus, the tunnel current is boosted.

As far as scalability is concerned, short channel effects (SCE) can also cause drain-induced barrier thinning and a degradation of the inverse subthreshold slope in a Tunnel FET just as in a normal MOSFET. As long as the channel is not too short which results in source-to-drain tunneling, a Tunnel FETs with SCE can still exhibit small off-state currents [AKB+08]. Another advantage of NW-based Tunnel FETs when scaling down is that the quantum capacitance limit is easier to reach since C_q is usually smaller than C_{ox} because $C_q \propto T_{WKB}$ [AKB+08].

1.4.3 Performance Boosters and State-Of-The-Art of Tunnel FETs

As already mentioned in the last section a material with a small bandgap at the source-channel tunneling point needs to be implemented to obtain a higher tunnel probability. Instead of a pure Si Tunnel FET, materials such as Ge or InAs with a smaller bandgap and smaller effective mass can be used as a source material. At the drain side a wider bandgap material or lower doping as discussed above is advantageous to hinder ambipolarity.

Ge as Source Material

There have been several studies on replacing the source with a different material such as Ge, both experimentally and by simulations [VVM+08]. Kim [KKHL09] used SOI planar technology and deposited poly-Ge in the etched away source region by CVD deposition to obtain a planar SOI Si Tunnel FET with Ge-source which is schematically depicted in Fig.1.11.

The source region overlaps the gate region to achieve vertical tunneling in the direction

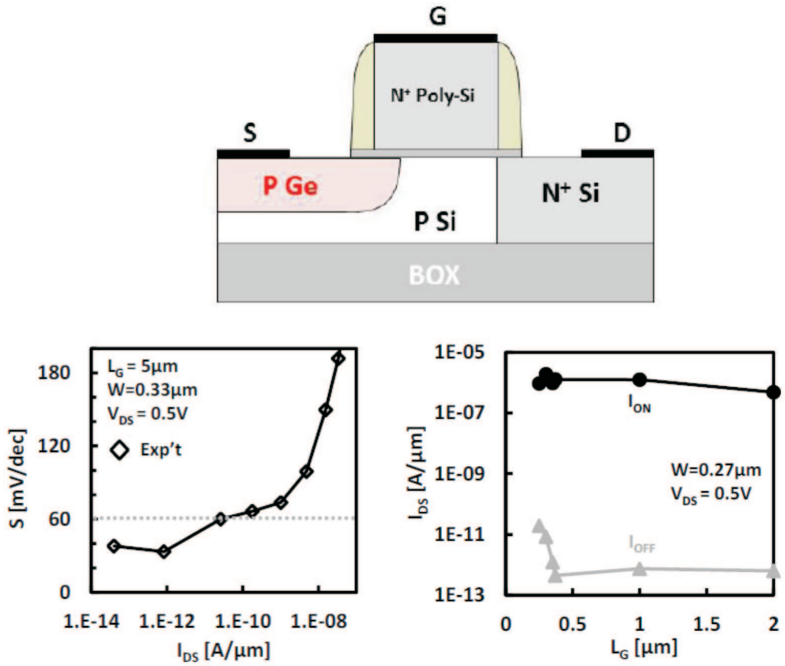


Figure 1.11: Schematics of a planar SOI Si Tunnel FET with Ge-source overlap with the gate. The corresponding inverse subthreshold slope as a function of drain current shows the characteristic bevahior of a Tunnel FET. An I_{on}/I_{off} ratio of 10^6 is reached. From [KKHL09].

perpendicular to the semiconductor/gate dielectric interface. A method used to obtain a larger tunneling area and, thus increasing the on-current as well as to improve process robustness

to process-induced variations stemming from gate-misalignment. Through the Ge-source and the given geometry for vertical tunneling the on-current was boosted to 0.42μA/μm and an I_{on}/I_{off} ratio of 10^6 at V_{DS}=0.5V was achieved [KKHL09]. Sub-60 mV/dec inverse subthreshold slopes were achieved over 3 orders of magnitude as shown in Fig.1.11. When the gate length is scaled below 400 nm with this device the leakage increases due to short channel effects (SCE). A limiting factor using this process is that between poly-Ge and Si an amorphous interfacial layer is seen which can be electrostatically considered as a larger resistor in series with the channel. This leads to weaker modulation of the tunnel barrier and likely to a higher inverse subthreshold slope at high drain current.

Low-Bandgap Materials at Tunnel Junctions

Another approach next to replacing Si in the source and drain are utilizing all III-V homo-junction and heterojunction Tunnel FETs. One issue in III-V homojunction Tunnel FETs is to obtain sharp junctions perpendicular to the growth direction. A vertical All-InGaAs Tunnel FET by Mookerjea [MMK+09] made use of high quality, in-situ doped junctions grown epitaxially by MBE. The structure is shown in Fig.1.12, having a gate length of 100 nm. The gate runs vertically along the channel and overlaps source and drain regions.

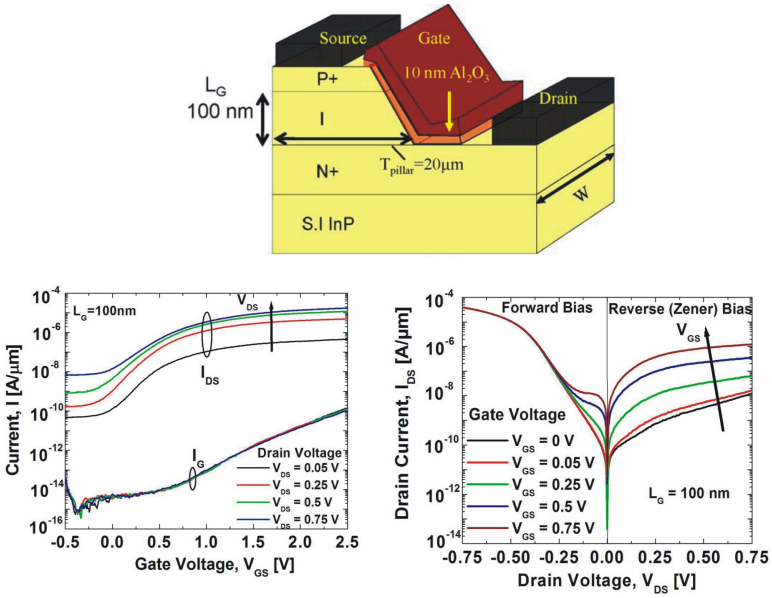


Figure 1.12: Schematics of a vertical InGaAs Tunnel FET. Transfer characteristics show an I_{on}/I_{off} ratio of 10^4 with an on-current of 20μA/μm at V_{DS}=0.75 V. Diode characeristics show NDR at room temperature. From [MMK+09]

Good device characteristics such as an on-current of 20 μA/μm at V_{DS}=0.75 V and NDR behavior at room temperature (see Fig.1.12) are demonstrated.

Heterojunctions

Unlike modulating the tunnel barrier by doping homojunctions, the use of heterojunctions allows for engineering the effective bandgap, i.e. the tunnel barrier. Different material systems are studied to provide optimal band alignment in a way such that the source material has a small effective bandgap to reduce the energy barrier at the source junction in the on-state. The drain material has a large bandgap to create a large energy barrier width on the drain side to keep off-currents low.

For III-V materials, owing to their small effective mass, either a staggered or broken gap

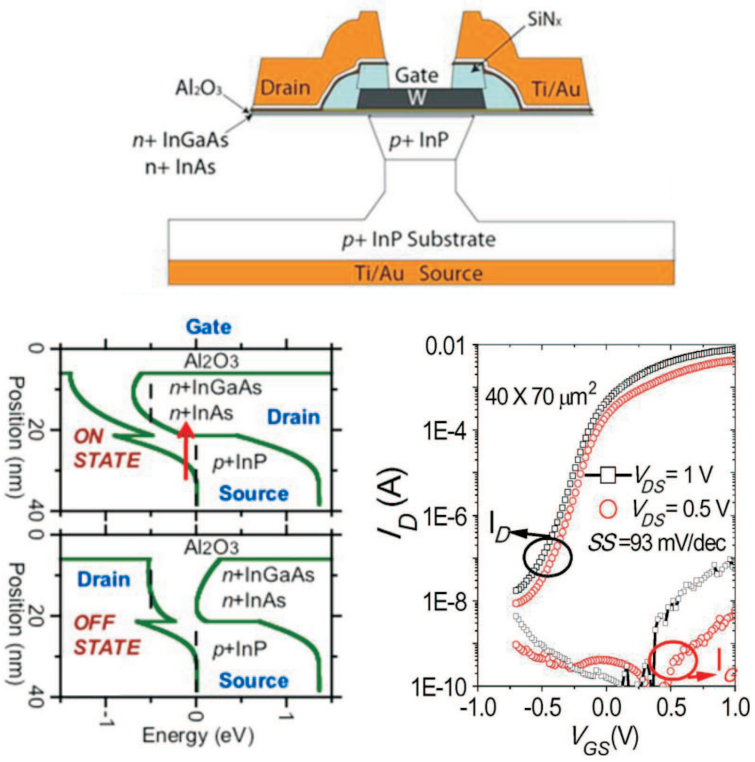


Figure 1.13: Schematics of a vertical InGaAs/InP Tunnel FET where the tunnel current runs normal to the gate, thus increasing the tunnel cross section. The band lineup during operation is shown below and the transfer characteristics on the right exhibit an inverse subthreshold slope of 93 mV/dec with an on current of 20 μA/μm at V_{DS} = 0.5 V and an I_{on}/I_{off} ratio of $6{\cdot}10^5$. From [ZLL+11].

are desired features to obtain a small effective bandgap which could lead both to a low subthreshold swing, high on current and high I_{on}/I_{off} ratios. Staggered and broken gap material systems with these features have been studied by Knoch and Appenzeller [KA10] and Koswatta [KKH10]. Zhou [ZLL+11] fabricated vertical n^+InGaAs/n^+InAs/p^+InP heterostructure Tunnel FETs. The cross section of such a vertical device is shown in Fig.1.13. The tunneling evolves normal to the gate at the n^+InAs/p^+InP tunnel junction to increase the tunneling cross section. The chemical composition of the InGaAs channel layer is graded from the n^+InAs tunnel junction interface to the InGaAs at the Al_2O_3 dielectric. Using a gate first approach with this configuration the gate dielectric-channel interface remains unaffected when etching undercuts for source and drain formation. The undercuts are passivated using SiN_x which is crucial to ensure low interface state densities. A high I_{on}/I_{off} ratio of $6 \cdot 10^5$ with a minimum inverse subthreshold slope S of 93 mV/dec is reported for the above structure. The on-current reaches 20 μA/μm at V_{DS} = 0.5 V. However, high interface state densities at the gate dielectric-channel interface and at the drain contact still remain. This hinders the inverse subthreshold slope to reach below 60 mV/dec. Another study on vertical III-V Tunnel FETs by Intel [DCKB+11] showed that a heterojunction achieves steeper S values due to a decreased source-channel tunnel barrier.

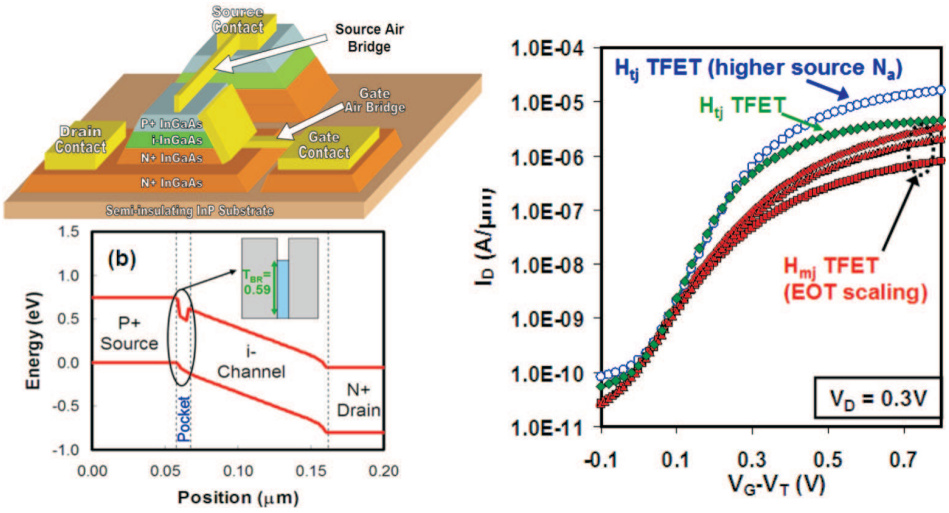


Figure 1.14: Schematics of a vertical InGaAs heterojunction tunnel FET utilizing a p^+-$In_{0.53}Ga_{0.47}As$/i-$In_{0.7}Ga_{0.3}As$/i-$In_{0.53}Ga_{0.47}As$ heterojunction with according energy band line up and transfer characteristics. A direct comparison between the heterjunction Tunnel FET and the p^+-$In_{0.53}Ga_{0.47}As$/i-$In_{0.53}Ga_{0.47}As$ homojunction Tunnel FET is made. The transfer characteristics of the heterojunction Tunnel FET with high source doping show an increase of 20x in on-current, compared to the homojunction Tunnel FET. From [DCKB+11].

A direct comparison between a p^+-$In_{0.53}Ga_{0.47}As$/i-$In_{0.53}Ga_{0.47}As$ homojunction and a p^+-$In_{0.53}Ga_{0.47}As$/i-$In_{0.7}Ga_{0.3}As$/i-$In_{0.53}Ga_{0.47}As$ heterojunction Tunnel FET was made. The device geometry is shown in Fig.1.14 together with the band lineup of the heterojunction Tunnel FET illustrating the effect of the thin i-$In_{0.7}Ga_{0.3}As$ pocket. The thin, 6 nm intrinsic $In_{0.7}Ga_{0.3}As$ pocket facilitates tunneling and improves the inverse subthreshold slope (green data points of the transfer characteristics in Fig.1.14) as compared to the homojunction Tunnel FET (red data points in Fig.1.14). Increasing the source doping further increased the on current by a factor of 20x (blue data points in Fig.1.14) for the heterojunction device.

A staggered heterojunction Tunnel FET utilizing a $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ tunnel junction [MBZ+12] and combined with EOT scaling has recently been shown to give very high on-currents and high I_{on}/I_{off} ratios. The on-current was 135 μA/μm at V_{DS} = 0.5 V with an I_{on}/I_{off} ratio of $2.7 \cdot 10^4$. Fig.1.15 illustrates the schemactics of the vertical Tunnel FET grown by MBE. GaAs- and InAs-like termination at the heterjunction was investigated to reveal that InAs termination gives the better heteroepitaxy which leads to the higher on-current.

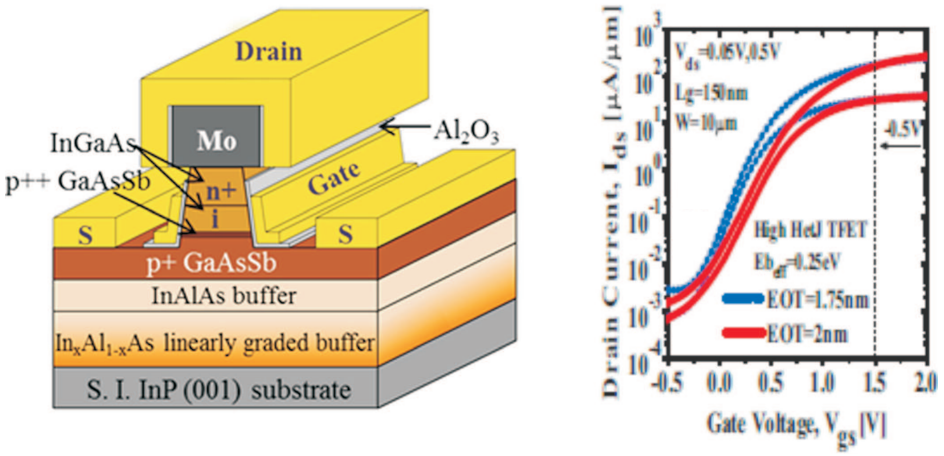


Figure 1.15: Schematics of a vertical staggered heterjunction tunnel FET utilizing a $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ staggered heterojunction with according transfer characteristics. The transfer characteristics of the staggered heterojunction Tunnel FET with scaling of EOT down to 1.75nm show an increase in on-current up to 135 μA/μm at V_{DS} = 0.5 V. From [MBZ+12].

The above experimental results give a short overview on state-of-the-art Tunnel FETs. It illustrates the many approaches which are currently being investigated and at the same time the challenges which current experimental Tunnel FETs face. Although most devices exhibit

low on currents (135 μA/μm at V_{DS} = 0.5 V) Tunnel FETs are promising for usage in low-power applications. The experimental results show that further EOT scaling, scaling of the body thickness as well as improved electrostatic control allow for further improvement of the on-current and lower inverse subthreshold slopes. Scaled heterostructure nanowires with scaled EOT offer a promising perspective for achieving low-energy switching.

1.5 Summary

The chapter started off by introducing scaling theory in CMOS which has been utilized over the past 40 years. Over the past 15 years scaling has become increasingly difficult due to SCE which prevent further lowering of the threshold voltage. The outcome is that leakage power makes up a significant portion of the entire power density. It was then shown that new ways have to be explored to retain the thermal limit of the inverse subthreshold slope S and at the same time scale down the supply voltage V_{DD}. Different approaches were presented such as the use of different geometries other than the conventional planar one to improve gate-to-channel coupling as well as the use of new channel materials. However, the use of optimized channel geometries along with high mobility materials does not suffice to further improve the I_{on}/I_{off} ratio.

Therefore, a device mechanism where the inverse subthreshold slope can be lower than the thermal limit of 60 mV/dec is needed to overcome the problem of scaling down the threshold voltage. Two different kinds of steep slope devices exist, one which amplifies the body factor m such as electromechanical FETs and ferroelectric FETs and the second type which changes the injection mechanism of carriers into the channel or induces an avalanche process to circumvent the thermal limit. Devices of the latter type are Tunnel FETs or iMOS .

Tunnel FETs are promising candidates to achieve inverse subthreshold slopes beyond 60 mV/dec and at the same time retain low leakage currents. The injection mechanism of Tunnel FETs is based on BTBT. The Esaki tunnel diode is a test structure to study BTBT. By studying device characteristics such as NDR behavior, PVCR, reverse tunneling current the quality of the tunneling junction can be explored. Further, different material systems can be combined to achieve a low effective bandgap which increases the tunneling current.

Different approaches to boost device performances in Tunnel FETs such as the on-current and inverse subthreshold slopes were presented. These were: replacing the source with a small bandgap material to enhance carrier injection into the channel and the use of heterojunctions to obtain a low effective bandgap.

2 Nanowire Growth and *in-situ* Doping

Two main processes are used to fabricate nanowires, namely the bottom-up and top-down approach. In this thesis only bottom-up approaches are utilized. All Si nanowires used in this work are grown with chemical vapor deposition (CVD) by the vapor-liquid-solid (VLS) method whereas all InAs nanowires are grown in a Metal Organic Vapor Phase Epitaxy (MOVPE) system by selective area epitaxy. This chapter gives an overview of the growth of Si and InAs nanowires as well as the *in-situ* doping mechanism. All nanowires were grown at IBM Research-Zurich by Dr. Mikael Björk and Heinz Schmid.

2.1 Si Nanowire Growth with VLS

All Si nanowires used in this work were grown in a chemical-vapor-deposition (CVD) chamber by the vapour-liquid-solid (VLS) growth mechanism [Wag70]. In the VLS mechanism metal nano particles or a thin metal film are deposited on top of the Si growth wafer. The wafer is then heated up in a CVD system to a temperature where the metal starts to melt forming small metal-Si alloy droplets. The precursor gas for the Si nanowires, Silane, is then inserted into the CVD chamber. The Silane preferentially cracks at the metal droplet surface allowing Si to incorporate into the droplet (Fig.2.1 A). Although a variety of different metals can be used [WSSG06][Wey78], Au is the preferred metal for VLS growth and used throughout this work [SSG05]. The Si supply from the gas phase causes the droplet to become supersaturated with Si (Fig.2.1 B). At first, the Si within the droplet crystallizes at the Si wafer/droplet interface and a solid crystal then precipitates out from the droplet leading to the growth of a nanowire (Fig.2.1 C). The solid crystal has a similar diameter as the deposited nano particles or droplets.

For the wires in this study gold colloidal particles having a diameter ranging from 20 to 60nm are used and deposited from a colloidal solution on a hydrogen-terminated Si [111] substrate. The hydrogen termination is achieved by a short dip in a buffered HF solution (BHF). In this work the growth is done, if not otherwise stated, at a wafer temperature of 450°C and a total pressure of 25 Torr using silane (SiH_4) diluted in Ar/He/H_2 to a partial pressure of 500 mTorr [SBK+08]. With these parameters typical growth rates of 25 nm/min are achieved. Since our nanowires are grown from colloids which have larger diameters than 20 nm, the growth direction of the nanowire is mainly directed in the [111] plane. This plane corresponds to the direction with the lowest interfacial energy. It has been shown elsewhere [SSG05] that for smaller diameters (<20 nm) the surface energy of the silicone nanowire determines the preferential growth direction. Fig.2.2 displays a SEM picture of a nanowire as well as a high resolution TEM picture showing the perfect single crystal structure.

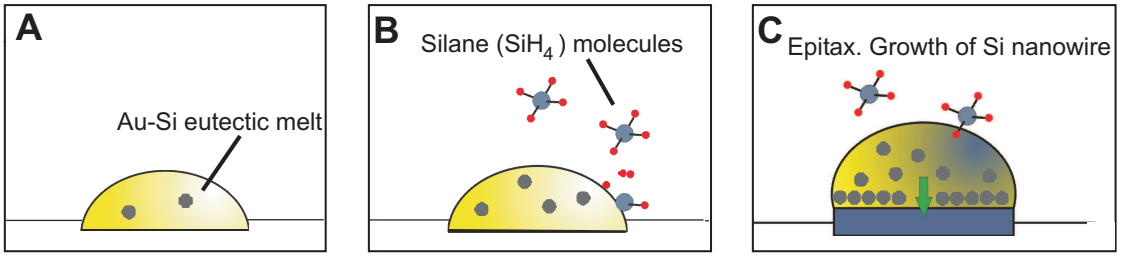


Figure 2.1: Au-Catalyzed Vapor-Liquid-Solid (VLS) growth: **(A)** Gold nanoparticles are annealed on Si substrates until an Au-Si eutectic melt forms. **(B)** Silane (SiH_4) is inserted into the reaction chamber which preferentially cracks at the gold surface. **(C)** Once super-saturation of the Au-Si eutectic melt is reached crystallization starts and epitaxial growth of the nanowire starts on the Si substrate.

2.1.1 *In-situ* Doping

Doping is an essential element to make an active device from a semiconductor. Control and manipulation of resistivity, contact formation and fabrication of device structures can be achieved by doping the semiconductor. In conventional planar devices doping is done by ion implantation. In this work ion implantation is utilized for some vertical devices as will be shown in the Processing section. To circumvent additional processing steps to implant desired regions of a nanowire and to hinder possible implantation damage to the nanowire, doping can be controlled already during nanowire growth, i.e. *in-situ*. This is done by introducing dopant gases along with the precursor gases needed for Si nanowire growth. To adjust the

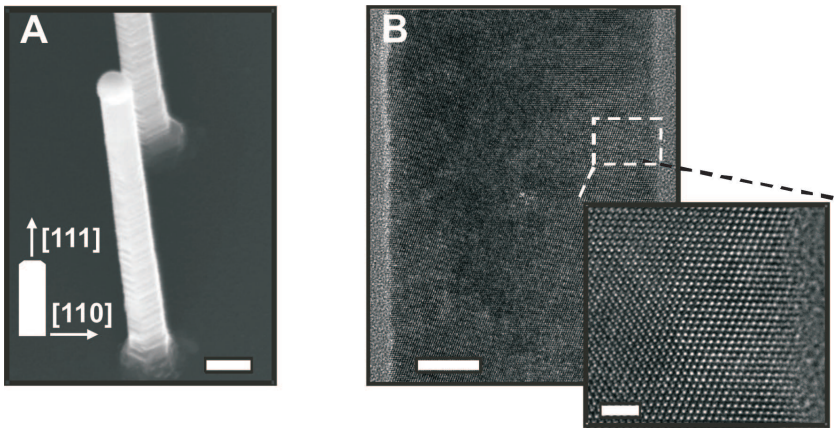


Figure 2.2: **(A)** SEM image of a VLS-grown silicon nanowire. Scale bar is 50 nm **(B)** TEM image of a silicon nanowire showing a perfect single crystal. Scale bar is 10 nm and 2 nm (inset).

doping level in the nanowire the gas flow ratio is set accordingly. With this technique phosphorous doping of Si nanowires has been achieved by several groups [ZLJL04] [WLH$^+$05]. A study [SBK$^+$08] performed in our group showed that n-type doping with phosphorous can be controlled from 1×10^{18}cm^{-3} to 1.5×10^{20}cm^{-3} which is the equilibrium solubility limit of P in Si at the given growth temperature (440°C). For p-type doping with boron practical doping densities up to 5×10^{18}cm^{-3} are reached which is limited by tapering of the nanowire resulting from amorphous boron-rich shell growth. The dopant precursor gases widely used are phosphine (PH_3) for phosphorous doping and diborane (B_2H_6) for boron doping. In this work 0.3% phosphine in He as well as 0.3% diborane in He was utilized for n- and p-type doping, respectively. By switching the precursor gases on and off during growth differently doped segments can be realized in a nanowire allowing for fabrication of *p-i-p*, *n-i-n*, *n-i-p* and *n-p* device structures. Along with the control of doping, the abruptness of doped segments is critical for device performance. It strongly influences the screening length which in turn affects the inverse subthreshold slope in scaled down devices. Although methods exist which measure dopants in nano-scaled structures such as atom probe microscopy, it is difficult to measure electronically active dopant distributions since only information on the chemical composition can be extracted. However, a new method utilizing TEM-based off-axis electron holography can measure directly the built-in potential of *p-n* or *i-n/p* junctions. This enables the determination of acceptor and donor concentrations. Using this method for *in-situ* doped nanowires grown in this work the junction abruptness of a i-n^+ junction was found to be between 7.5 nm and 30 nm per decade of carrier concentration.

VLS-grown Si nanowires used throughout this work, having diameters around 60 nm, were grown with high n-type doping densities and abrupt junctions by *in-situ* doping. This allows to fabricate different device structures such as *p-n* and *p-i-n* structures for Tunnel FET devices which will be shown in the Results section. A general issue with VLS-grown nanowires is the contamination with gold from the droplet during growth. The solubility of Au in the semiconductor poses serious concerns since during synthesis Au might be incorporated into the nanowires creating deep level traps which are highly detrimental to the electronic transport [LGMJ80] [TP83] and degrades junction quality in devices such as FETs and Tunnel FETs. Another important aspect of gold contamination is that it remains on the surface of the Si nanowire posing challenges during further processing. Au can catalyze a series of chemical reactions of silicon with wet chemicals, dry process gases, or even at ambient atmosphere. These challenges and their implications on device processing will be studied in details in the Processing section 3.2.2.

2.2 Catalyst-Free Growth of InAs Nanowires

Silicon as the channel material has limitations in the maximum obtainable effective velocity when scaling down below the 45 nm node [KA08] which is given by the low channel mobility. Using new channel materials with high mobilities at low electric field leads to high injection velocities in scaled devices (see section 1.2.2). III-V materials such as InAs for n-channels and Ge for p-channels are widely being investigated to substitute Si. For heterojunction tunnel FETs, III-V materials such as InAs are of interest as source material. The focus in this work is on InAs nanowires with its superior material properties over silicon. Unlike the Si nanowires studied here, InAs nanowires in this work are grown without a catalyst particle by Metal Organic Vapor Phase Epitaxy (MOVPE). MOVPE is a method to grow/deposit thin solid films on solid substrates using organometallic compounds as precursor sources. This technique was first demonstrated by Manasevit in 1968 [Man68]. Nanowires are grown without catalyst particles by selective area epitaxy in an MOVPE system. This is done by locally growing through a patterned mask (typically SiO_2 or Si_3N_4) deposited on a semiconductor substrate. Precise vertical orientation and perfect positioning at predetermined sites, all in a controlled manner, is possible and Au contamination is not an issue as in the case with Si nanowires. The geometry of nanowires gives not just ideal electrostatic control, it also enables the epitaxial combination of different materials into heterostructures. Growing heterostructures as planar

films is restricted by the stability for thick layers (several μm) where the limit of mismatch growth is in the range of several 0.1% strain. Going above this limit leads to strain and defect formation in thin films. For nanowires the strain is relieved elastically by changing the relatively small cross section [ZH99]. There have been several studies on selective area epitaxy: Motohisa and Mohan [MNT+04], [MMF05] were among the first to study selective area growth of GaAs, InGaAs and InP nanowires grown selectively on ⟨111⟩B oriented substrates of the same material as the nanowires. Tomioka [TMHF08] showed selective area growth of InAs nanowires on ⟨111⟩ Si substrates having a mismatch-strain of 11.6 %. Although a high density of point defects is present directly at the Si-InAs heterointerface, the defects do not propagate into the wires [RVW+06], [BBS+11].

For all InAs nanowires grown here 2" ⟨111⟩ Si and ⟨111⟩B InAs substrates were masked with a 65-nm-thick SiO_x layer deposited by (PECVD). Subsequently mask openings to the substrate surface were fabricated by electronbeam lithography and oxide etching in buffered hydrofluoric acid (BHF) (Fig.2.5). As precursors tertiary-butyl-arsine (TBAs) and trimethyl-indium (TMIn) are utilized. The details of the growth setup are explained in Appendix A.1. Growth

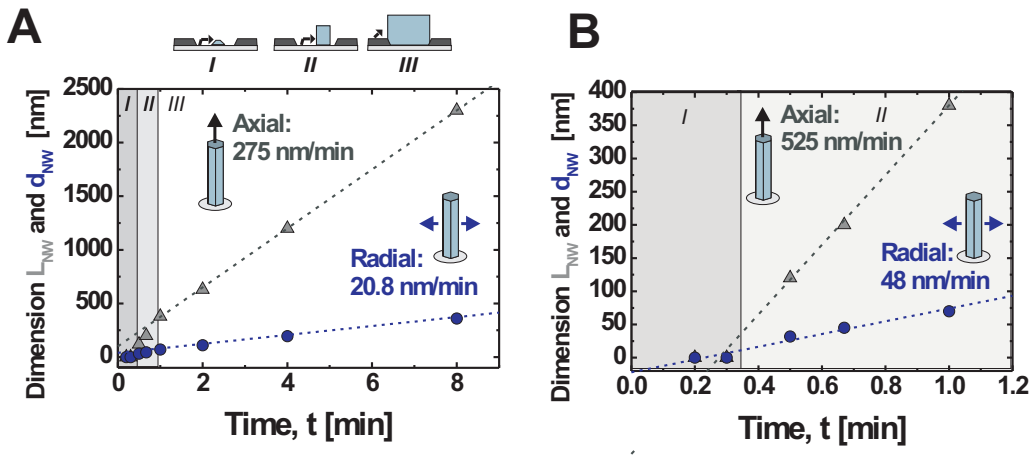


Figure 2.3: Different growth phases for InAs selective area epitaxy growth: **(A)** Overview of 3 growth phases. Phase I: Nucleation of an InAs cluster within the mask opening. Phase II: In supply coming mainly from the open Si area. Phase III: In supply coming from the vapor/oxide mask. **(B)** Close-up of Phase I and II which shows an axial growth rate of 525 nm/min and a radial growth rate of 48nm/min. From [BSB+12]

is done at a substrate temperature of 520°C. The axial ⟨111⟩ and radial ⟨1-10⟩ InAs nanowire growth is dependent on various growth parameters and can be altered by varying growth conditions such as duration, temperature, group-III molar flows, V/III ratio, mask material, mask opening size, and inter-wire distance [BSB+12]. As has been shown in a detailed growth

study by our group [BSB+12] the growth on Si substrates takes place without an In droplet and the process evolves through three successive phases as shown in Fig.2.3 A. In the first phase the nucleation of an InAs cluster takes place, followed by two distinct nanowire growth phases where the two growth phases have different axial and radial growth rates. These two phases originate by a transition from having In supply dominated by the open Si area in the phase II towards an In supply from the vapor/oxide mask in the growth phase III. In phase III an axial growth rate of 275 nm/min and a radial growth rate of 20.8 mm/min is observed. A close-up in Fig.2.3 B shows the two distinct growth rates in phase II being 525 nm/min for axial growth and 48 nm/min for radial growth. The spacings between mask openings have an

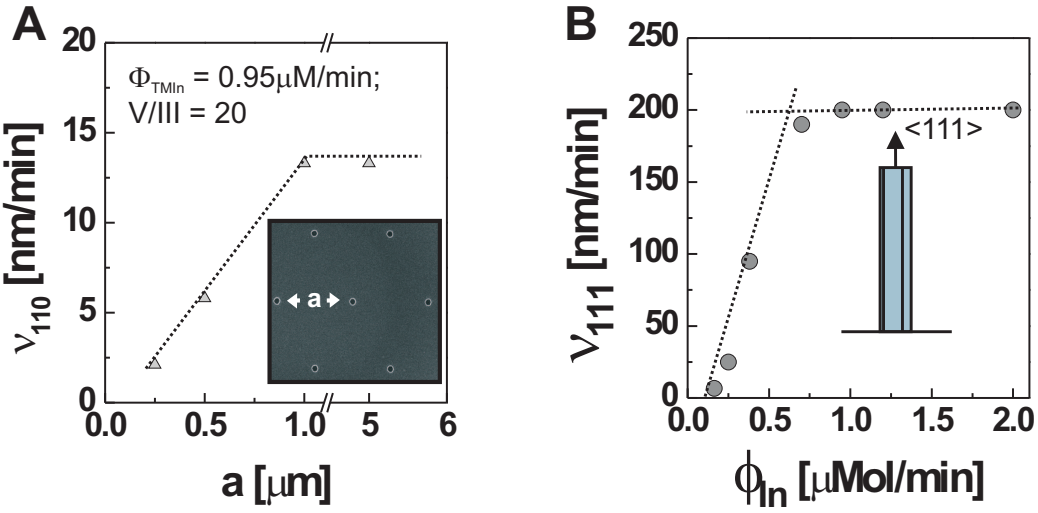


Figure 2.4: **(A)** Mask opening spacing **a** vs. radial growth rate. The inset shows an SEM image of the SiO_2 mask openings after BHF etch. **(B)** Axial ⟨111⟩ growth rate as a function of TMIn flow during growth. Two distinct growth regions are seen, at low and high In flow. From [BSB+12]

influence on the radial growth rate as shown in Fig.2.4 A. Two distinct regions of high radial growth at large spacings and low radial growth at small spacings are observed. In the case of small spacings a reduced In supply from the substrate to the mask opening is likely the cause for a smaller radial growth due to competing nanowires close by. Large spacings allow more In supply from the substrate and this then leads to an increase of the radial growth rate. As will be shown in section 5.2.2 altering of the TMIn flow leads to two distinct growth regions as a function of TMIn flow which affects the incorporation of dopants into the nanowire. In Fig. 2.4 B the axial growth rate is shown as a function of the TMIn flow during growth. At high In flow (Fig.2.4, points on the right) the V/III ratio is locally higher in the mask openings [BSB+12] which does not change the morphology or composition of the InAs nanowire. All

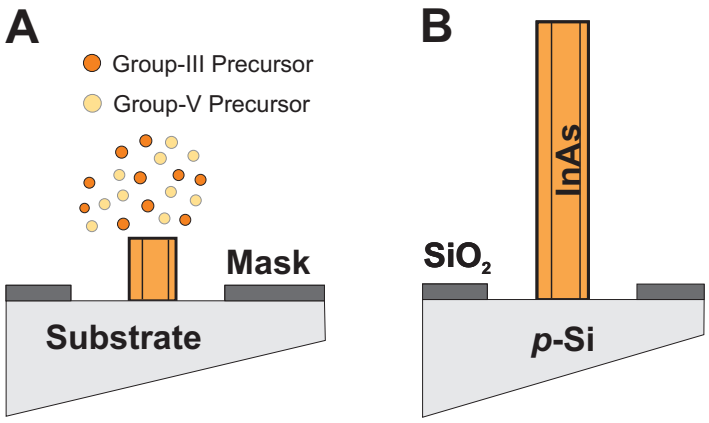


Figure 2.5: Selective Area Epitaxy on Si substrates: **(A)** Group III and V percursors are thermally cracked at the substrate surface and epitaxial growth evolves through three successive phases **(B)** Fully grown InAs nanowire. The diameter depends on growth conditions and mask design.

InAs nanowires in this work which are grown on Si substrates are broken off after growth for lateral electrical contacting on a different substrate. Therefore, a dense hexagonally assembled array (5000×5000 openings) with 150 nm wide openings being 1 μm apart from each other is chosen. Because the wires are placed in a large and dense array the ⟩1-10⟩ (radial) growth rate is suppressed in favor of the ⟩111⟩ growth rate. Fig. 2.5 depicts the schematics of the InAs nanowire growth on Si substrates for large arrays. Hereby an initial cluster is formed within the mask opening, followed by epitaxial growth of the nanowire (2.5A). After growth the nanowires have lengths of approx. 3 μm and diameters in the range of 100 to 150 nm. The initial diameter at the beginning of the growth is retained(2.5B). This method is therefore ideal for growing samples to study doping since the radial growth is diminished and, thus, uniform doping can be achieved.

In the case when InAs nanowires are grown directly on p-type ⟨111⟩B InAs substrates for Tunnel devices, the growth mechanism differs from that on Si substrates. ⟨111⟩B is the preferred growth direction for vertical InAs nanowires. In this case, the precursor material fills the entire opening and can even exceed the opening (Fig.2.6A). Due to the wider spaced mask openings for single vertical Tunnel diode devices the ⟨1-10⟩ (radial) growth is not entirely suppressed and the grown nanowires are in the range of 200-400 nm with initial 150 nm wide openings (Fig.2.6B).

Fig. 2.7 shows an SEM picture of a nanowire array and single nanowires growing on ⟨111⟩ Si substrates. All nanowires exhibit a hexagonal cross section with {110} facets and smooth sidewalls (Fig. 2.7 (B) and (C)). Growth was done at 520°C substrate temperature at a TMIn

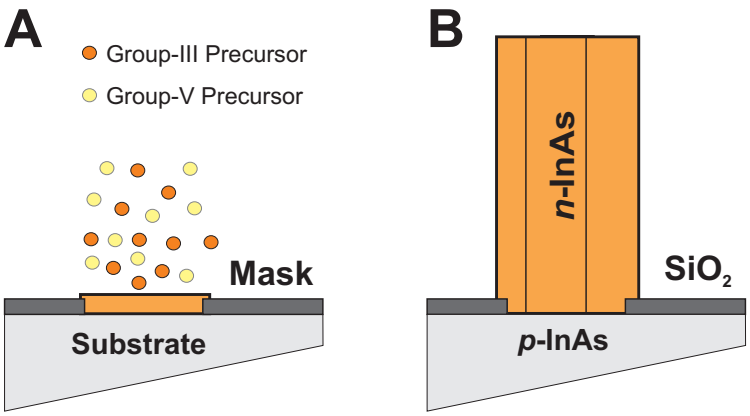


Figure 2.6: Selective Area Epitaxy on InAs Substrates: **(A)** Group III and V percursors are thermally cracked at the substrate surface and epitaxial growth begins within the entire mask opening. **(B)** Fully grown InAs nanowire. The end diameter depends on growth conditions and mask design. In this case no dense array is used and therefore the nanowire fills out the entire mask opening.

molar flow of Φ_{TMIn} = 0.38 μMol/min and a V/III precursor flow ratio of 20 unless stated otherwise. Under these conditions an axial growth rate of ~ 50 nm/min is obtained.

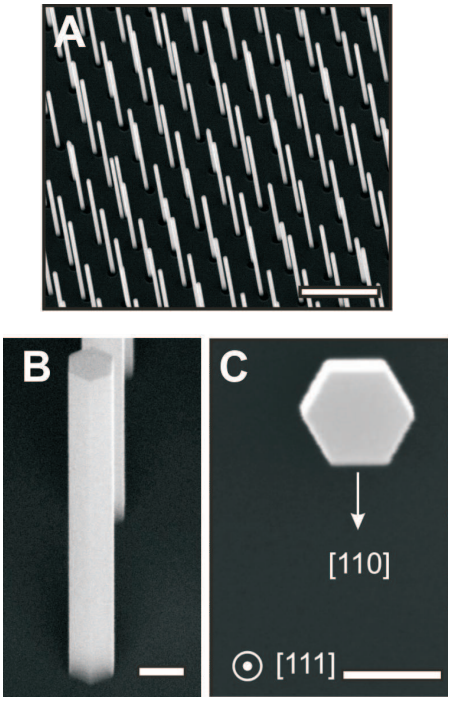


Figure 2.7: **(A)** SEM picture of an InAs nanowire array and single nanowire **(B)**, both taken under 30° angle. **(C)** single InAs nanowires from a top view. Scale bars are 2μm, 200 nm and 200 nm, respectively.

2.2.1 *in-situ* Doping

Controlled doping is required for altering the electrical properties of a semiconductor and for fabricating devices such as e.g. Tunnel diodes and Tunnel FETs. For InAs nanowires grown by the VLS-mechanism with Au-catalyst, there have been several n-type doping studies with a variety of dopants (Sn, Se, S, Si, Te) [ASK+10] [TDB+10]. Due to the pinning of the Fermi level 0.1 eV above the conduction band, p-type doping is not possible. Remote p-type doping has been, however, achieved by growing p-doped InP shells around VLS-grown InAs nanowires [LWB+07]. There has only been Si doping reported so far [WWW+11] for InAs nanowires grown with selective area MOVPE . This section describes the method used to incorporate dopant atoms during MOVPE growth, i.e. *in-situ* without a catalyst. Several dopant species are studied and the resulting electrical characteristics as well as the influence of dopants on the morphology of the nanowire will be discussed in the Results section. Uniform doping is desired along the nanowire axis as well as the radial direction. Unintentional doping, often referred to as background doping, stemming from the TMIn and TBAs precursors in the form of C is always present. The amount of unintentional C incorporation has been shown to depend on growth temperature and In precursor type [TDB+10]. As dopant precursors organometallic compounds and hydrides are commonly used. The effectiveness of incorporating dopants is dependent on many parameters during growth such as group-III/V and doping precursor type, precursor ratio (III/V ratio), growth temperature, pressure and flow rate. The parameter which describes the effectiveness of incorporation is the **compositional distribution coefficient K_C** [Str89]:

$$K_C = \frac{x_D^s}{x_D^g} = \frac{x_D^s}{(P_g^D / P_g^V)} \tag{2.1}$$

where x_D^s is the fraction of group-V sites in the solid occupied with dopants (when n-type dopants in InAs are considered) and x_D^g is the ratio of doping precursor and group-V precursor molecules in the gas phase (Fig.2.8). As will be shown in section 5.2.2 a change in the precursor flow ratio changes the incorporation of some dopant species.

In this work only *n*-type doping incorporation into InAs nanowires is investigated. During growth and with the same conditions as described before either diethyl telluride(DETe), disilane (Si_2H_6), hydrogen sulfide (H_2S), or carbon tetrabromide (CBr_4) was injected into the

chamber together with the InAs precursors. The flow of the dopant precursors is changed with respect to the flow of the In and As precursors and varied accordingly. The flow ratio of dopant precursor to InAs precursors $\Phi_{dop}/(\Phi_{TMIn}+\Phi_{TBAs})$ ranged from 10^{-5} to 10^{-2} and growth was done at a substrate temperature of 520°.

Overall, the growth conditions obtained in the previous chapter allow for homogeneous lengths and diameters which is essential to achieve uniform dopant incorporation and abrupt junctions for Tunnel diode devices. As will be shown in section 5.2.2 a variety of dopant species is studied with the goal to achieve uniform and high enough doping as well as exact control of n-type doping concentrations which are a prerequisite to obtain high tunnel currents in Tunnel diodes and eventually in high performance Tunnel FETs.

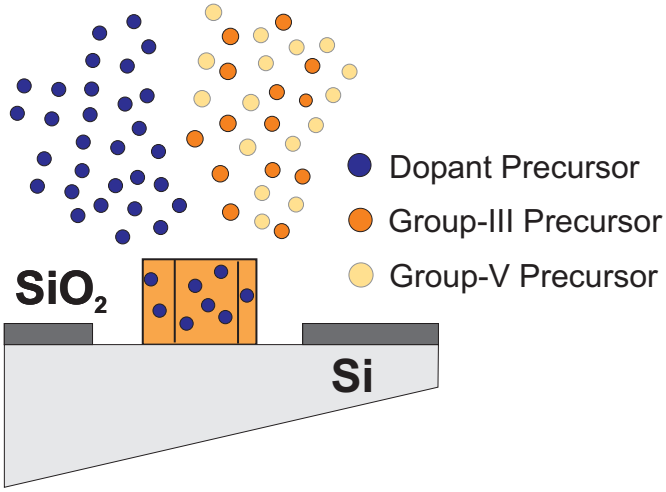


Figure 2.8: Schematics of *in-situ* doping. During growth either diethyl telluride(DETe), disilane (Si_2H_6), hydrogen sulfide (H_2S), or carbon tetrabromide (CBr_4) is injected into the chamber together with the TMIn and TBAs precursors and the flow ratio is varied from 10^{-5} to 10^{-2}.

2.3 Summary

This chapter introduced the nanowire growth techniques utilized for Si and InAs nanowires. The dopants utilized throughout this work are described and how they incorporate within the nanowire crystal is shown. Table 2.1 summarizes the properties of VLS growth used here for Si nanowires and MOVPE growth for InAs nanowires. The use of VLS-grown nanowires can lead to Au contamination during device fabrication, whereas with MOVPE growth no contamination occurs. The high selectivity of the radial and axial growth rate make it easier to grow long nanowires without modulation of the diameter. MOVPE growth enables easy positioning of nanowires which makes it easier integrate into devices. However, the radial growth rate for MOVPE grown InAs nanowires strongly depends on the growth conditions and a change in the TMIn flow leads also to a change in dopant incorporation, as will be shown in section 5.2.2.

Table 2.1: Properties of VLS and MOVPE growth

Property	**VLS**	**MOVPE**
Material	Si	InAs
Precursors	SiH_4	TBAs,TMIn
Doping Precursors	n:PH_3, p:B_2H_6	n: Si_2H_6, H_2S, DETe, CBr_4
Growth Temperature	450°C	520°C
Position Control	none	mask
Nanowire Diameter	size of Au particle	growth conditions

3 Device Fabrication

In this chapter the fabrication of all single nanowire devices studied in this thesis will be presented. Single nanowire devices can be fabricated in two geometries: the lateral and the vertical geometry. The term lateral here means that the nanowires are "plucked off" from their growth substrate and put on a different substrate for further processing. The nanowires lie on top of the substrate, thus the orientation to the substrate is lateral. In the vertical geometry the nanowires are grown vertical and kept on the growth substrate and processing is done on the same substrate; keeping their vertical orientation as well as always being in contact with the growth substrate. The lateral geometry is suitable for resistivity measurements as less processing steps are needed, compared to the vertical fabrication. Physical properties such as nanowire and contact resistivities can be determined, as well as the junction quality of p-n or p-i-n junctions. As devices lateral single nanowire diodes and Tunnel FETs in a top-gate configuration are fabricated . A disadvantage of the lateral geometry is that the top-gate does not wrap around the entire circumference of the nanowire as this would involve more complex processing to etch away the substrate underneath the nanowire and deposit gate dielectric and gate metal uniformly around the nanowire. The vertical geometry has the advantage that the gate wraps around the entire nanowire, enhancing gate control over the channel. From a technological point of view, the vertical geometry is preferred since, along with the capability of vertical integration, the growth substrate serves as a contact to the nanowire device.
In the following, all processing steps for lateral and vertical devices are presented and discussed.

3.1 Lateral Devices

Following the nanowire growth as described in chapter 2, nanowires are transferred from the growth substrate to a Silicon wafer covered with SiO_2 for electrical contacting of single nanowires. The oxide is primarily used to isolate the nanowire from the substrate electrically. However, if a voltage is applied to the backside of the substrate, the influence of back-gating effects on device characteristics can also be studied. As shown in Fig.3.1 a piece of cleanroom cloth held by hand with tweezers is used to mechanically break off the nanowires from their growth substrate and place them onto the oxide-covered silicon wafer by gently sweeping the

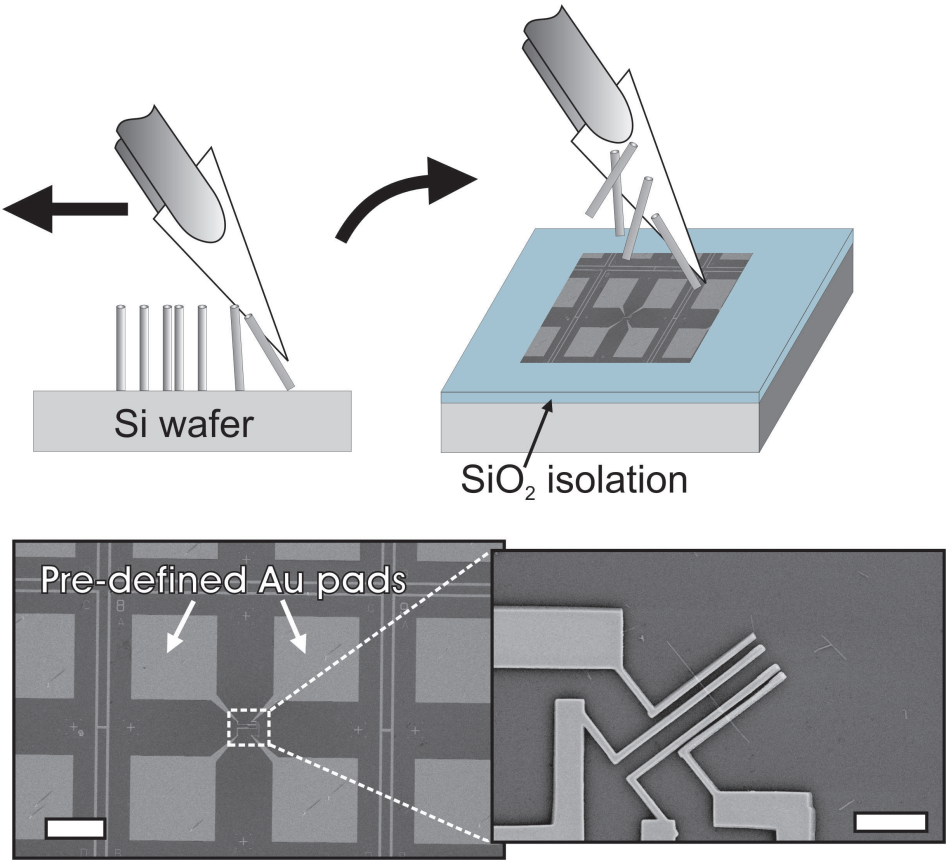


Figure 3.1: Schematics of transferring nanowires from the growth substrate to the device substrate for lateral processing. A cleanroom cloth held by hand with tweezers is used to mechanically break off the nanowires from their growth substrate and place them onto the oxide-covered silicon wafer by gently sweeping the cloth. The Si device wafer has photolithographically pre-patterned Au pads serving as contact electrodes. An SEM image of Au pads and a close up of a nanowire connected to the big pads by contact leads is shown. The contact leads were fabricated by electron beam lithography, metal evaporation and lift-off. Scale bar is 4 μm and 2 μm, respectively.

cleanroom cloth across. The Si wafer has photolithography pre-patterned Au pads serving as contact electrodes to the nanowires. An SEM picture with the Au pads and a close up of a nanowire which is connected to the pads by contact leads written with electron beam lithography is also shown in Fig.3.1. All lateral devices, either 2-point, 4-point probe or 3-terminal devices, are contacted in this way.

3.1.1 2-and 4-Point Contact Structures

For lateral Si or InAs devices used for 2-point or 4-point probe measurements, the nanowires were mechanically transferred from the growth substrates to degenerately doped *p*-type Si substrates (0.002 Ωcm). The substrate was covered with a 100-nm-thick thermal SiO_2 layer and pre-patterned Au pads, as discussed before. A thin layer of about 300 nm of PMMA electron beam resist was spun on the substrate and baked at 175°C for 2 min. The Au pads, serving as contacting pads for probes during measurement, were also used as a guide to optically record the position of the nanowires and pattern two or four contacts to each individual nanowire by electron-beam lithography. For all electron beam exposures a dose of 170 $\mu C/cm^2$ with a 10 μm aperture was used. After electron beam exposure and developing the PMMA resist in isopropanol/H_2O (7:3) for 45 s, a short O_2-plasma cleaning was carried out to remove any resist residues. Then the sample is dipped in BHF for 5 s and is subsequently loaded into an evaporation chamber, where 70 nm Ti and 80 nm Au or 150 nm Ni were evaporated, if not stated otherwise. For *in-situ* doped p-n or p-i-n Si nanowires two contacts were patterned to the nanowire. For single InAs nanowires four contacts with the spacings between the electrodes varying from 120 nm to 650 nm were patterned to perform 2-point transmission line measurements and 4-point probe measurements. After electrical measurements, SEM images were recorded to obtain the nanowire diameter and the distance between contact leads for the data analysis. An SEM picture of a finished InAs contact structure is shown in Fig. 3.2 together with the measured resistance as a function of electrode spacing and a 4-point probe measurement. All 2-point and 4-point probe measurements are performed under ambient conditions or in a flow cryostat with an Agilent Parameter Analyser B1500 A.

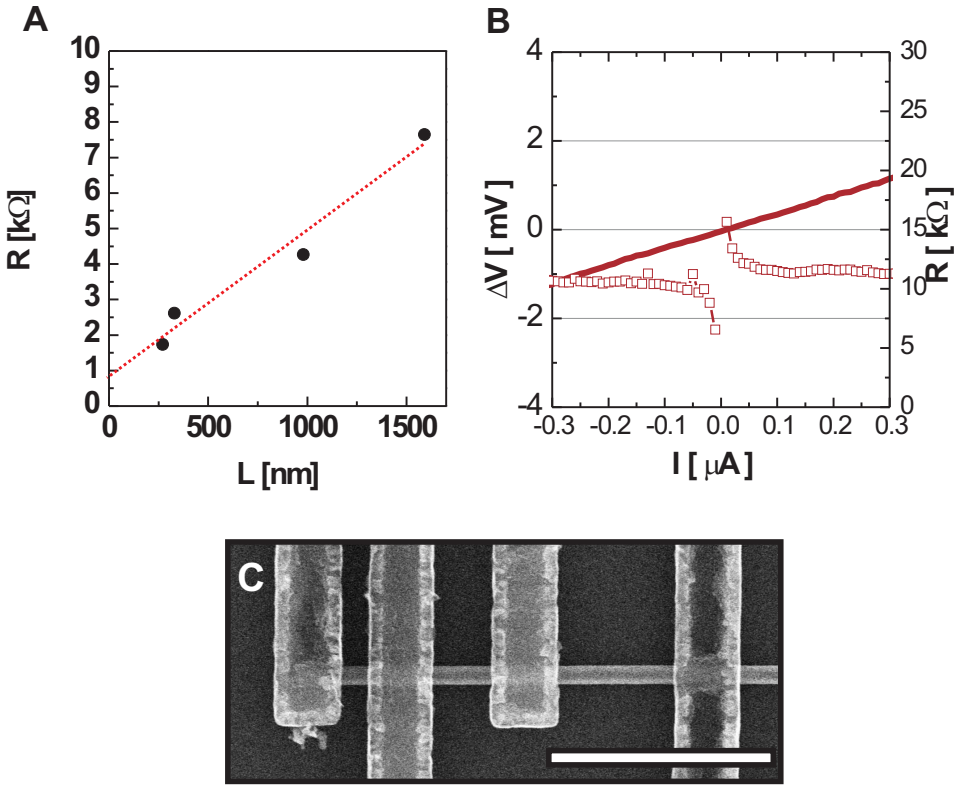


Figure 3.2: **(A)** 2-point measured resistance as a function of electrode spacing of a single InAs nanowire contact structure. **(B)** 4-point probe measurement of the same structure. Solid line corresponds to the measured voltage drop ΔV, the squares to the resistance R. **(C)** SEM picture of the measured nanowire contact structure. Scale bar is 1 μm.

3.1.2 3-Terminal Devices

For lateral 3-terminal devices Si nanowires were *in-situ* doped during growth. The goal was to obtain p-i-n structures to serve the fabrication of Tunnel FETs. *In-situ* doping was chosen over implantation and other methods because implantation can damage the crystal structure of the nanowire. Additionally, after implantation an activation anneal is needed which can further damage the crystal structure. Another reason is the higher complexity of the process: two independent implantation runs are necessary after the nanowire has been transferred to the device substrate, one for implanting n-dopants and one for p-dopants with two additional electron beam lithographies to isolate the region to be implanted. Other doping methods such as spin-on-glass or diffusion doping from a doped oxide also need additional processing steps and a high temperature anneal to drive in and activate the dopants. This can lead to poor junction quality due to smearing out of the junction. The finished device is a top-gated

structure with source and drain contact on each end of the nanowire; over the n and p region. The gate covers the entire intrinsic part. The device is fully isolated to the substrate by a 100 nm thick thermal silicon oxide to avoid any leakage paths. In this way the substrate can also be gated, grounded or left floating.

The fabrication process of two different device structures is described in the following: a device with a SiO_2 gate dielectric and one with HfO_2. The goal is to study the influence of a high-κ gate dielectric on device performance and compare this to devices having a SiO_2 gate dielectric. As both oxides are deposited by a different method, each process flow has to be adapted which will be shown in the following.

SILICON OXIDE GATE DIELECTRIC

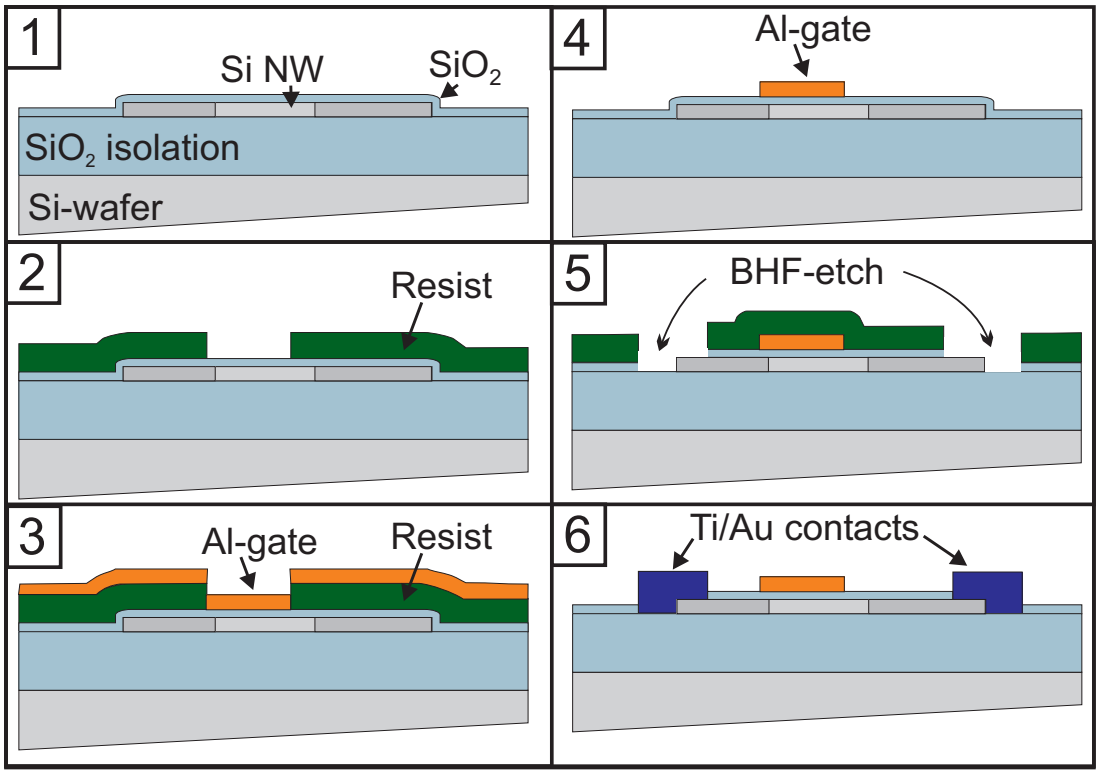


Figure 3.3: Schematics of the process flow for lateral Si Tunnel FETs with SiO_2 gate dielectric: **(1)** Deposition of SiO_2 Gate Dielectric by PECVD. **(2)** Gate lithography by electron beam. **(3)** Evaporation of Al for the gate metal. **(4)** After gate lift-off. **(5)** Second lithography by electron beam for the source/drain contacts. Before evaporation of Ti/Au contact metal, the gate dielectric is etched away in the contact area by BHF. **(6)** Finished device after contact metal evaporation and lift-off.

Determining Nanowire Coordinates

As has been already shown in Fig.3.1 *p-i-n* Si nanowire structures are transferred from the growth substrate to the device substrate. It is pre-patterned with Au pads and markers for contacting the nanowire as well as to record the position of single nanowires. The recording is done by taking an optical image and determining the position of the nanowire relative to an Au pad array. This is done by a home-made Labview program. Due to tapering on the p-side of the *p-i-n* structures as explained in section 2.2.1, the p-side can be discriminated from the n-part in the optical image. Knowing at which end the n-and p-segment is and knowing the lengths of all segments from the growth parameters, the position of the intrinsic segment can be roughly determined. The accuracy of recording the nanowire coordinates is determined in the accuracy of locating the nanowire relative to the Au pad markers in the optical image. Once the coordinates are known an electron beam mask is designed for the source/drain contact leads and the gate to the nanowire.

Gate Dielectric and Electron Beam Lithography of Gate Stack

When it comes to choosing the right gate dielectric for the lateral Si Tunnel FET devices, deposition/growth temperature of the oxide as well as etch rates and etching selectivity have to be considered. As already mentioned, high temperature processes should be avoided due to diffusion of dopants smearing out the junctions. A high quality thermal oxide can therefore not be used as gate dielectric. We choose a PECVD SiO_2 which can be deposited at low temperature ($\sim 300°C$) and still give reasonable electrical quality. The schematics of the process for the Tunnel FET device with SiO_2 gate dielectric is depicted in Fig.3.3. A 20 nm SiO_2 is then deposited over the wafer in an Oxford PECVD chamber (Fig.3.3 (1)). The chamber temperature is kept constant at 300°C. To ensure a uniform and reproducible deposition, a dummy run is executed before the actual wafer is let in the chamber. For processing the top gate a 300 nm thick PMMA resist is first spun on the sample and baked at 175°C for 2 min on a hotplate. The gate pattern is then written with an electron beam as well as the contact leads from the gate to an Au pad (Fig.3.3 (2)). The gate alignment is critical and influences the electrical device characteristics. It is limited by the inability to exactly locate the intrinsic region. After development of the PMMA in isopropanol/H_2O (7:3) for 45 s and a short O_2-plasma cleaning step the wafer is mounted in the metal evaporation chamber and 120 nm Aluminium are evaporated (Fig.3.3 (3)). The excess Aluminium together with the PMMA resist

is lifted-off in Acetone, resulting in the schematics as shown in Fig.3.3 (4).

Contacting the Nanowire

For the source and drain contacts, once again PMMA resist is spun on, followed by electron beam exposure for the contact area as well as the leads to the pads and subsequent development, as discussed above. A short O_2-plasma is done before immersing the substrate into a buffered oxide etch solution to etch away the PECVD SiO_2 gate dielectric in the contact areas (Fig.3.3 (5)). Subsequently, the wafer is loaded immediately into the evaporation chamber and 8 nm Ti and 110 nm Au are evaporated. The schematics of a finished device after lift-off is seen in (Fig.3.3 (6)). An SEM image of a finished lateral p-i-n^+ nanowire Tunnel FET is also shown in Fig.3.4.

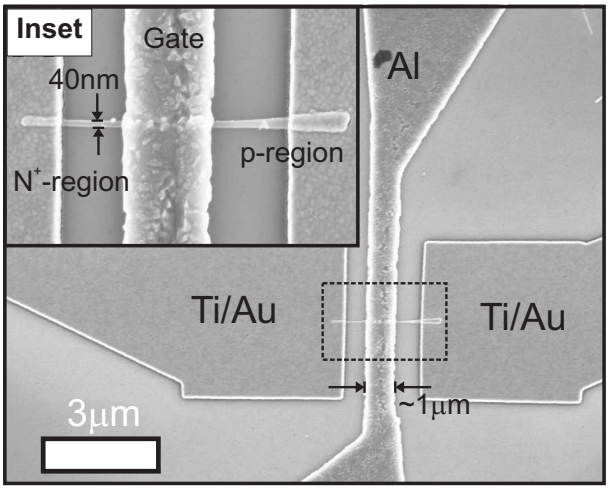


Figure 3.4: SEM image of a tunnel FET device with source/drain and gate contacts. The inset in the upper left shows a close-up of the NW Tunnel FET. The p-type end can be identified as the tapered region.

HfO_2 GATE DIELECTRIC

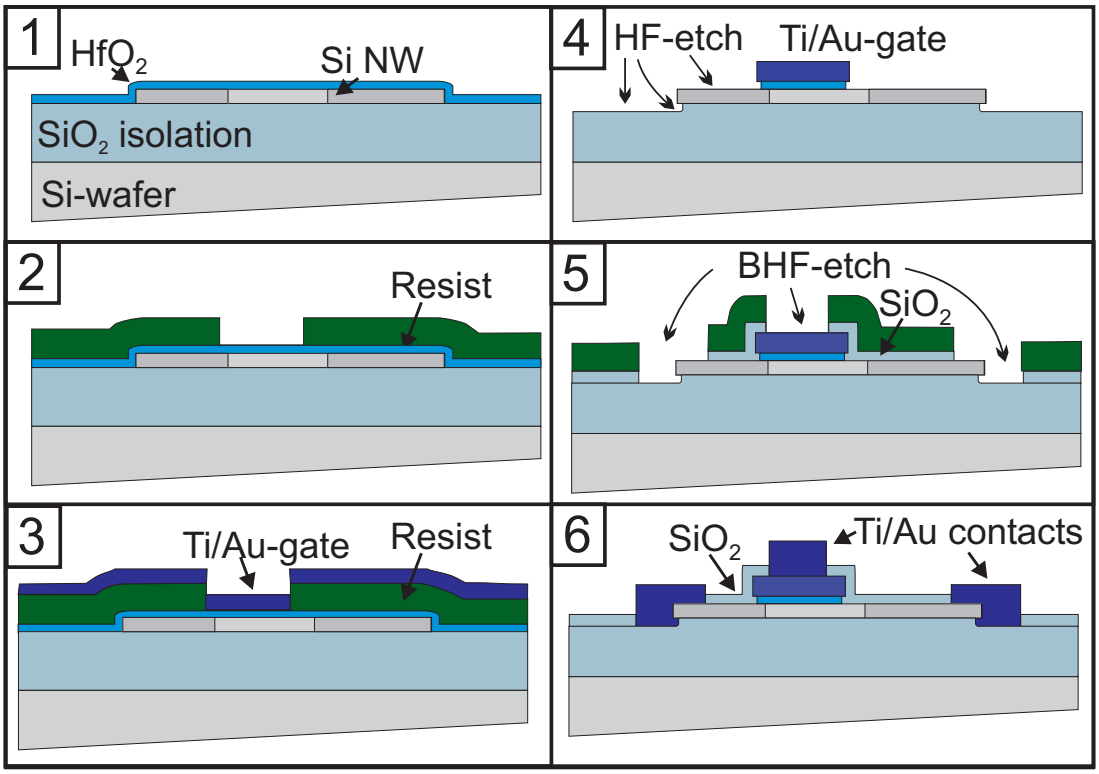


Figure 3.5: Schematics of the process flow for lateral Si Tunnel FETs with HfO_2 gate dielectric: **(1)** Deposition of SiO_2 gate dielectric by PECVD. **(2)** Gate patterning by electron beam lithography. **(3)** Evaporation of Al for the gate metal. **(4)** Schematics after processing the gate. **(5)** Second lithography by electron beam for the source/drain contacts and gate opening. Before evaporation of Ti/Au contact metal, the gate dielectric is etched away in the contact area by BHF. **(6)** Schematics of the finished device after contact metal evaporation and lift-off.

HfO_2 Gate Dielectric Deposition

When using HfO_2 as gate dielectric, the lateral process introduced before for a SiO_2 gate dielectric has to be adapted. Here, the HfO_2 is deposited by ALD at a temperature of 250°C. If HfO_2 is deposited at a higher temperature than 250°C, it becomes very difficult to etch in BHF or HF solution or even impossible to remove. The reason for this is crystallization and densification which makes the HfO_2 film highly resistant to wet etching. Here, 5 nm of HfO_2 are deposited by ALD at 250°C (Fig.3.5 (1)). The HfO_2 was deposited at Lund University by C. Thelander.

Etch Selectivity of HfO_2 to SiO_2

Crucial for the process is the selectivity of etching HfO_2 towards SiO_2. HfO_2 has a lower etch rate than SiO_2 in buffered HF or dilute HF solutions. It thus requires longer etch times to remove the same thickness. A problem of having long etch times is that HF creeps under the electron beam patterned PMMA film. Thus, the oxide does not only get etched in the open areas but also in the surroundings under the etch mask leading to unwanted etching of the gate dielectric or even lift-off of the PMMA mask. To reduce the etch time a higher concentration of HF could be utilized. But higher concentrated HF solutions have a SiO_2:HfO_2 etch selectivity of 50:1 or even higher which would lead to uncontrolled etching of the underlying isolation oxide when etching the contact area (see Fig.3.3 (5)). To circumvent this, we developed a process where the HfO_2 is etched in a strongly diluted HF solution (0.5%) after gate patterning. The solution has an SiO_2:HfO_2 etch selectivity of nearly 1:1 which solves the selectivity problem.

Gate as a Hard Mask for Etching HfO_2

The patterning of the gate follows the same process as for the SiO_2 gate dielectric. Here, the gate is used as a hard mask which solves the issues of diluted HF creeping underneath the resist mask. The HfO_2 is etched away in diluted HF solution except under the patterned gate (see Fig.3.5 (4)). The HF solution is diluted in deionized (DI) H_2O to 0.5%. As the HF etches Aluminium, a Ti/Au gate metal is used instead. The HF solution etches slightly the gate dielectric around the edges of the gate and into the isolation oxide, as indicated in Fig.3.5 (4).

Contacting the Nanowire

Before patterning the source/drain contacts 20 nm of PECVD SiO_2 is deposited to isolate the region between the gate and source/drain contact (Fig.3.5 (5)). Then, the source/drain contacts are patterned together with the gate once more to open up the gate contact area. Before evaporation of the contact metal, the 20 nm thick PECVD SiO_2 is etched away in BHF solution in the contacts and gate area as seen in Fig.3.5 (5). The finished device is schematically shown in Fig.3.5 (6).

The main difference between the HfO_2 and SiO_2 process is due to the etch selectivity. To goal is to study the influence of the different gate stacks using the same batch of grown nanowires. The gate with the high-κ gate oxide should improve the performance of the Tunnel FET which

will be shown in section 4.1.3.

3.2 Vertical Devices

This section describes the processing flow which was developed for vertical InAs homojunction tunnel diodes and vertical Si FETs. The general schematics for vertical 2-point tunnel diodes and 3-terminal devices is shown in Fig.3.6. In Fig.3.6 (A) the top part of a single InAs nanowire serves as the source contact and is isolated to the substrate by a spacer layer. As all vertical devices are connected to their growth substrate, the back side of the substrate can be used as a drain contact. For vertical Si FETs the drain and source are the top and back side contact, respectively. The gate wraps around the intrinsic part and part of the doped region of the nanowire. It is isolated to the top source contact by a spacer layer (Fig.3.6 (B). A SiO_2 isolation oxide on top of the substrate together with the deposited gate dielectric inhibits leakage between the gate and substrate. In the vertical geometry the gate can not be self-aligned onto the intrinsic part of the nanowire as in the lateral CMOS case. Several process steps need to be developed to set the gate height correctly across the intrinsic region. First, the process steps for fabricating vertical InAs homojunction tunnel diodes will be explained, followed by the process flow of vertical Si FET devices.

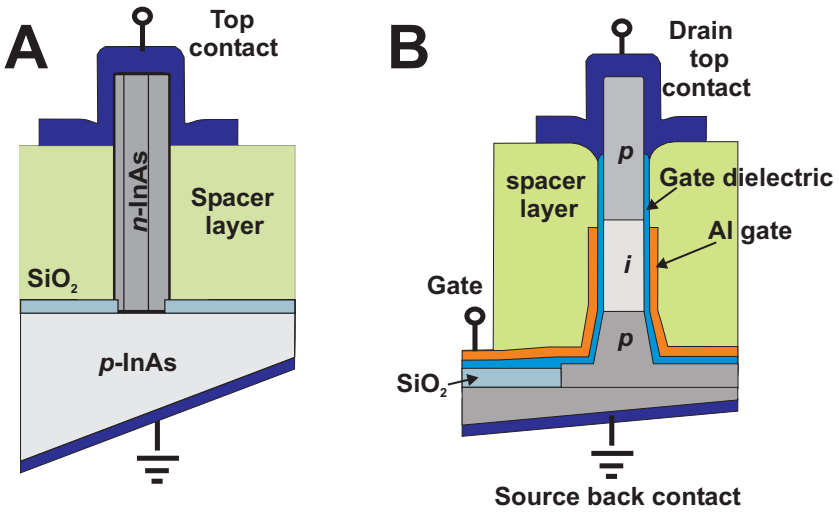


Figure 3.6: Schematics of vertical devices: **(A)** Vertical tunnel diode structure for InAs nanowires. The top contact serves as source and the substrates as drain contact. **(B)** Vertical Si nanowire FET. The top contact serves again as source with the bottom contact at the substrate as drain. The gate is wrapped around the entire intrinsic region of the Si nanowire. It is isolated from the source by a spacer layer and from the substrate by SiO_2.

3.2.1 Tunnel Diode Devices

The growth of vertical InAs nanowires is described in section 2.2. For tunnel diodes a different growth mask was used than the hexagonally patterned openings for lateral devices. Here, single openings spaced large enough (several 100 μm) apart in order to contact a single nanowire are utilized. The substrates used for homojunction tunnel diodes are epi ready ⟨111⟩B *p*-InAs wafers. As mask material a 65 nm thick PECVD silicon oxide is deposited on the wafer. Using the same growth conditions as before nanowires were grown to a length of about 1 μm. After growth, a layer of benzocyclobutene (BCB) was spin-coated onto the wafer, completely encapsulating the wires followed by an O_2/SF_6 reactive-ion etch to etch back the BCB layer and reveal the top 300 to 500 nm of the InAs nanowires. Optical lithography was used to define top contacts to the individual diodes, and after a brief oxide etch in BHF, 25 nm of Ti and 100 nm of Al were evaporated to form the metal contacts. Ti/Al was also used for the metallization of the back side of the wafer to form the common drain contact. Fig. 3.7 shows the schematic of such a diode device and an SEM picture of the metal pad contacting the top of the nanowire (seen as the white spot in the middle of the circular pad in Fig. 3.7 B).

The resulting nanowire fills the entire mask opening and once it reaches the surface of

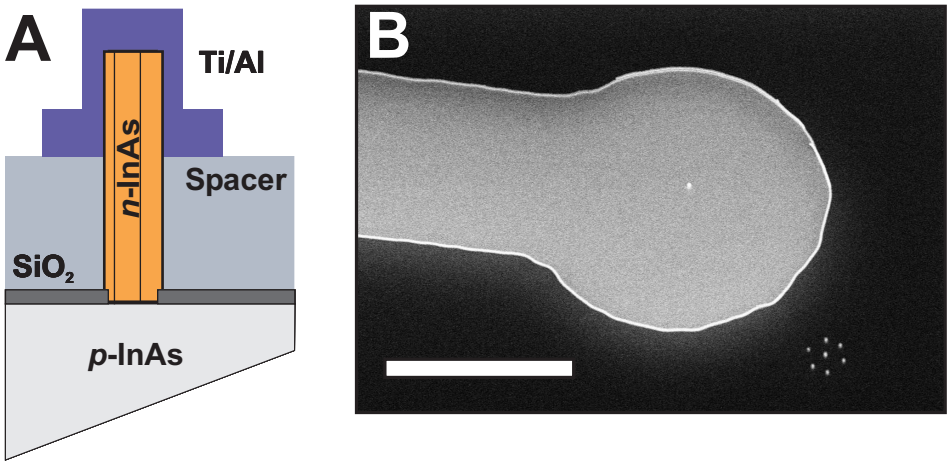


Figure 3.7: **(A)** Schematic cross section of a vertical tunnel diode **(B)** SEM of the top metal pad to contact the nanowire (The top of the nanowire is seen as a white spot in the middle of the pad), scale bar is 2 μm

the oxide, the radius further expands (Fig.3.8 A). Fig.3.8 B shows a single diode after the BCB polymer was back-etched. Craters can be seen around the nanowire. The conducting nanowire sticking out of the BCB layer acts as an antenna enhancing the electric field around it during the RIE etch. These craters, however, don't reach the substrate surface to cause shorts.

After the measurements of some devices it is necessary to know the exact diameter at the substrate-nanowire interface for data analysis. Before growth when the mask is etched it is not possible to determine the exact diameter in the SEM due to the risk if contaminating the substrates. Therefore, after measurement the top contact metal was wet-etched, followed by etching away the BCB layer in RIE and finally wet-etching the entire InAs nanowire. SEM inspection then reveals the exact diameter of the mask opening of a specific device (Fig.3.8 C). The variation of mask openings was between 280 nm to 310 nm.

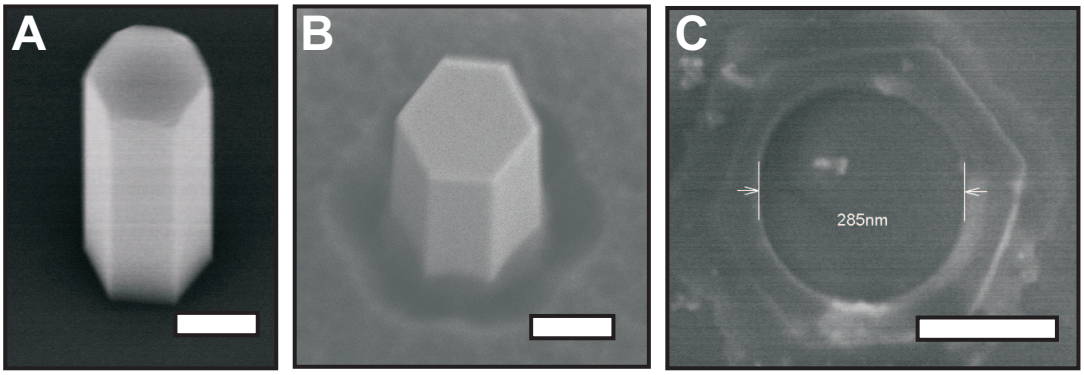


Figure 3.8: SEM pictures of **(A)** a grown vertical InAs nanowire, **(B)** the nanowire embedded in the BCB spacer layer and **(C)** the mask opening in the oxide after etching away the top contact, BCB spacer layer and the InAs nanowire to reveal the true contact size to the InAs substrate. Scale bars are all 200 nm.

3.2.2 Three-Terminal Devices

Three-terminal devices in the vertical architecture studied here consist of p-i-p or n-i-n structures for pFETS or nFETs, respectively. To fabricate single nanowire devices, the nanowires have to be isolated from others during processing or positioned accordingly to avoid several nanowires within the device area. This is particularly challenging for Si nanowires, because they are grown by VLS with gold colloids as catalysts (see growth chapter) and are therefore not positioned by a growth mask on the substrate, as in the case for vertical InAs nanowires grown by selective area epitaxy.

Two schemes to isolate single nanowires have been tested as presented in Fig.3.9:

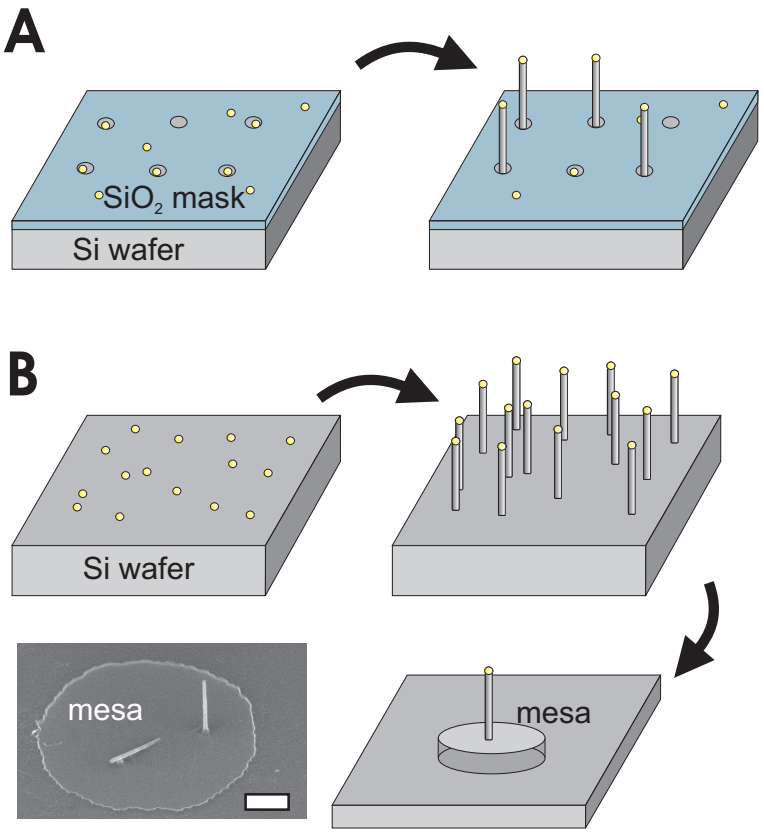


Figure 3.9: Nanowire growth using an oxide mask *vs* random growth and mesa etch **(A)** Au colloids or immersed over an oxide covered substrate with hole openings. By adapting the colloid concentration the density of colloids on top and within the hole openings can be controlled. After growth the oxide is stripped, leaving only nanowires grown in the hole openings. **(B)** Au colloids are randomly dispersed on top of the substrate. After growth a mesa is etched out of the substrate, leaving only nanowires which are located on top of the mesa. By adjusting the mesa size and colloid concentration before growth in average one nanowire per single mesa circle can be obtained. An SEM image of the mesa structure with a single standing nanowire on top is shown at the bottom left. Scale bar is 300 nm.

Masked Growth

The masked growth method utilizes an oxide mask where hole openings are written with electron beam lithography and etched in BHF (Fig.3.9 (A)). Different hole sizes as well as colloid concentrations are tested. Before nanowire growth Au colloids are immersed on top of the mask which then either stay on top of the oxide or in the hole openings. After growth the oxide is removed with BHF together with the remaining Au colloids on top of the mask, leaving only the nanowires grown within the hole openings. Although this approach allows to specifically position nanowires on the substrate, the yield of actual nanowires growing out of the hole openings is very low. Often, the colloids don't assemble in the opening or assemble at the oxide wall at the edge of the opening.

Random Growth

Here the colloids are randomly dispersed on top of the ⟨111⟩ Si growth wafer. The nanowires grow randomly on the subtstrate. After growth mesas are etched into the substrate, etching away all nanowires which are not covered by the etch mask. By controlling the size of the mesa structures as well as the colloid concentration the density of nanowires can be controlled to a point where mostly only one nanowire is present on each mesa structure. The size of the mesa is chosen to be 6 μm diameter.
Due to the low yield of nanowires with masked growth the random growth approach is used here for fabricating vertical devices ((Fig.3.9 (B)).
In order to make a transistor structure out of a vertical nanowire the top (and bottom) parts needs to be highly doped since these parts will be the source and drain regions of the transistor. Because the growth wafer serves also as the drain back contact, a highly degenerate p-or n-type wafer is utilized for nanowire growth. As in the lateral case, the doping of the top part can in principle be done by introducing dopant gases during the growth. The main problem is that under the conditions for epitaxial growth with high yield of vertical wires without defects the introduction of high concentrations of doping gases causes instabilities in the growth and leads to kinks along the length of the wires. For lateral devices, this was not severe, since the nanowires are plucked off the growth substrate and placed on the device substrate. This can be done several times until the desired yield is reached on the device substrate. Furthermore, as discussed before, achieving p-type doping is difficult due to tapering by an overgrowth of

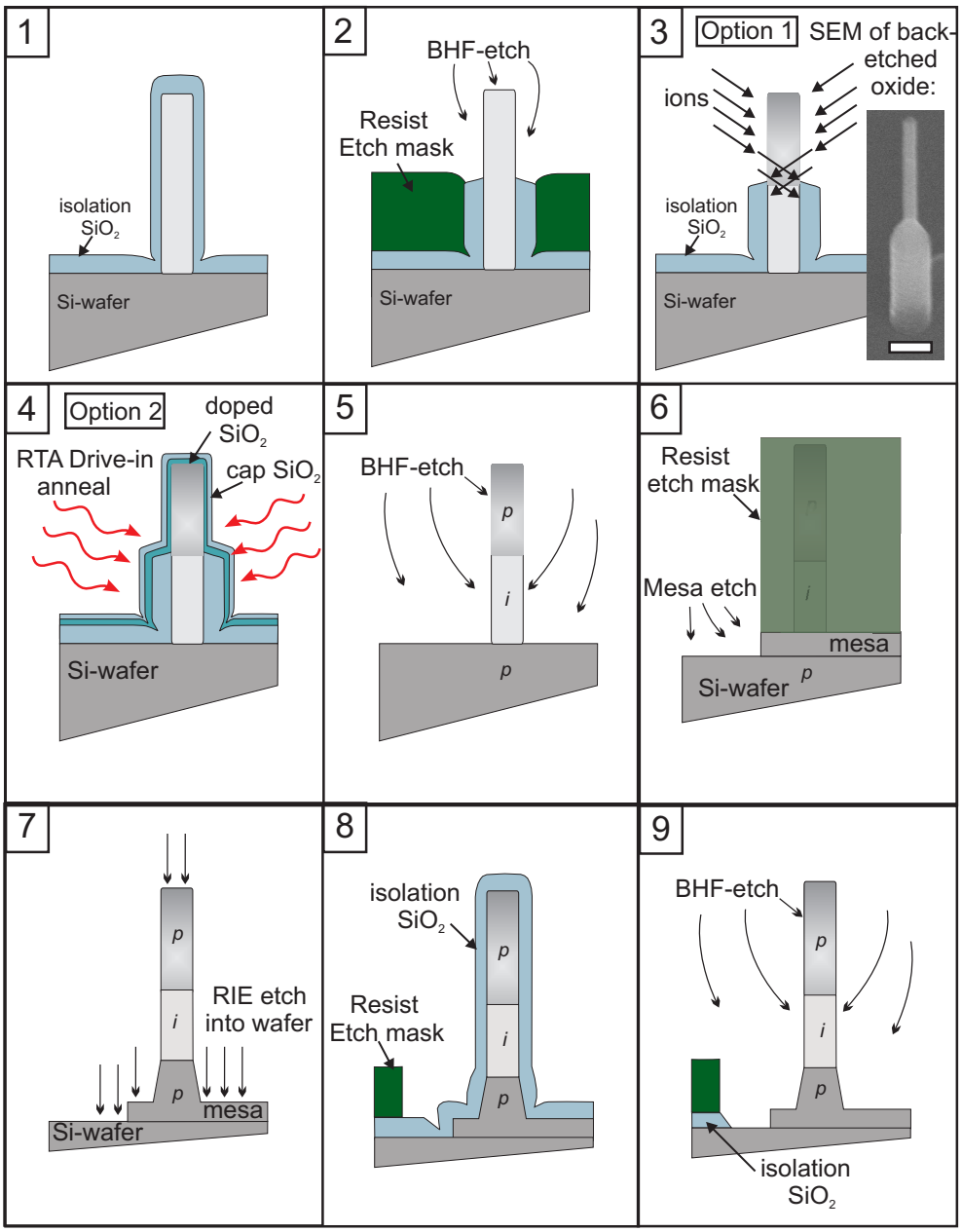


Figure 3.10: Schematic of process flow for vertical Si devices - doping of top part and isolation. **(1)** & **(2)** After growth the nanowires are covered in PECVD oxide and resist followed by an anisotropic back-etch of the resist in O_2 plasma. This frees the top part. After etching the oxide away of the exposed top part in BHF solution, the substrates are either **(3)** implanted with boron ions (Option 1) or **(4)** a heavily phosphorous doped oxide is deposited followed by a drive-in of the dopants from the oxide into the top part of the nanowire (Option 2). Scale bar in SEM image is 200 nm. **(5)** All oxide is removed in BHF afterwards. **(6)** Isotropic mesa etching, followed by **(7)** an anisotropic etch into the substrate. **(8)** & **(9)** Isolation oxide to isolate mesa from the rest of the wafer. The next steps are depicted in Fig.3.12.

an amorphous Boron-rich shell. Therefore, when utilizing *in-situ* doping for vertical devices the yield of vertically aligned nanowires is still very low on the growth substrate. This requires other routes of introducing dopants into the wires, such as implantation and diffusion doping. In the following, all process steps are explained in detail as well as process issues are discussed which arise during fabrication. At the end of this section an improved process flow is presented which addresses the process issues.

Removal of Au Catalyst Particles After Growth

The Au colloid used for VLS growth is remaining on top of the nanowire after growth as shown in Fig.2.2. As Au can cause several chemical reactions during device fabrication with etching solutions, the Au colloid has to be removed. For this, the substrate with the vertical nanowires is immersed after a short HF:H_2O (1:5) dip in KI/I_2 solution etching away the gold catalyst from the top of the nanowires.

Implantation of Top Part

The next step is to prepare the wafer for doping of the nanowire top part. As only the top part should be doped, the rest of the nanowires have to be shielded. This is done by first depositing 100 nm PECVD SiO_2 resulting in about 50 nm of oxide on the side walls of the nanowires as shown in Fig.3.10 (1). UV resist is then spin coated onto the wafer and anisotropically etched with O_2 plasma in an Oxford RIE system revealing the top part of the oxide-covered nanowires, which is shown in Fig.3.10 (2). The oxide on the top is etched away in BHF solution (7:1 mixture of Ammonium Fluoride and 50%HF) and the resist stripped in Acetone. For implantation, the ion dose and energies have to be adapted to the nanowire geometry to avoid implantation damage in the crystal structure. For p-type doping, Boron is commonly used in Si, whereas for n-type doping, Phosphorous or Arsenic can be used. Calculations have been made for each dopant type to assess the implantation depth at a given acceleration energy. Furthermore, the implantation is done at a tilt angle of 45° from four orientations with 90° steps. With this approach the total dose can be split into four and thus any damage to the crystal structure is reduced. The process is depicted in Fig.3.10 (3) and Fig.3.11 (A). For Boron, the calculated projected penetration depth is 11 nm at 2.5 keV. To achieve the same depth for Phosphorous

ions, an energy of 8 keV is needed and even higher for Arsenic because these atoms are heavier. As these high energies are not favourable, only Boron dopants are considered here for implantation into the nanowire. The total dose during implantation is 4.5×10^{14} cm^{-2} which gives a calculated doping concentration of $\approx 10^{19}$ cm^{-3}. A fast fourier transform analysis (FFT) of a high resolution TEM image (Fig.3.11B) was used to evaluate crystalline disorder in the nanowire. The high resolution TEM (HRTEM) picture shows an as-grown and as-implanted nanowire without annealing. The implanted and non-implanted portions are both single crystalline as shown in the inset. After implantation a high temperature anneal is performed to activate the dopants in the nanowire crystal in a rapid thermal annealer (RTA) for 10 s at 950° C under H_2/Ar atmosphere.

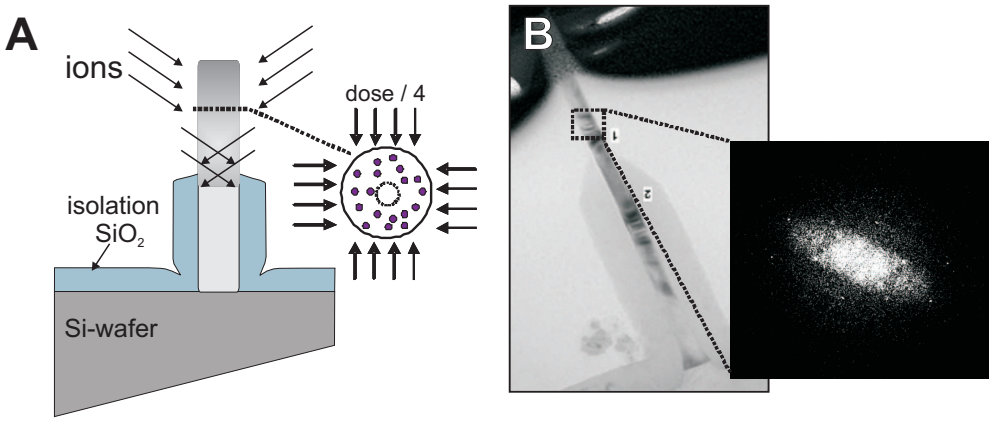


Figure 3.11: Implantation with boron ions of top part of nanowires. **(A)** Schematics showing the implantation at an angle of 45° from four orientations with 90° steps to reduce damage of the crystal structure. The total dose during implantation is 4.5×10^{14}cm^{-2}. **(B)** FFT analysis of HRTEM images were used to evaluate crystalline disorder in the nanowire. HRTEM showing an as-grown and as-implanted nanowire without annealing. The implanted and non-implanted portions are both single crystalline as shown in the inset. Courtesy: Y. Zhu, G. Cohen, S. Bangsaruntip, IBM Watson Research Lab.

Diffusion Doping of Top Part

Due to the limitation of implanting n-type dopants as discussed above, n-i-n structures are fabricated instead by diffusion doping of the top part of the nanowire. The nanowires are covered with a 20 nm thick highly phosphorous doped PECVD SiO_2 followed by 40 nm of capping oxide as depicted in Fig.3.10 (4). The wafer is then annealed in an RTA at 950°C for 60s which makes the dopants diffuse from the oxide into the nanowire. With this technique

doping concentrations of $9.6{\cdot}10^{19}$ cm^{-3} are achieved.

Isolation of Single Nanowires

After the drive-in or implantation all oxide is stripped off in BHF solution (Fig.3.10 (5)). The next step is to isolate a single nanowire by etching the mesa. This is done by defining circular and alignment structures by photolithography and isotropic reactive ion etching with SF_6 (Fig.3.10 (6) and Fig.3.9). The mesa is approximately 60 nm high and 6 μm in diameter after the resist is stripped and all nanowires outside the mesa are etched away. After a cleaning step involving a short O_2 plasma and short BHF dip a second unmasked anisotropic RIE step is used to etch 100 nm vertically into the substrate as shown in Fig.3.10 (7). This is needed to align the gate onto the *p-i* or *n-i* interface at a later stage. Since the etching is strictly vertical towards the substrate it also etches unwanted kinked nanowires on top of the mesa away. A cleaning step in O_2 plasma and a short BHF dip is then done to remove the Teflon coating on the nanowire originating from the anisotropic etch.

Field Isolation

To hinder any leakage currents from gate and source contact pads to the substrate which can cause shorts to the drain, an isolation layer outside of the mesa area has to be deposited. First, a 100 nm isolation field oxide is deposited by PECVD which wraps the entire surface of mesa, nanowire and wafer. UV resist is then spin coated on and the mesa revealed by photolithography with the same mask as used when etching the mesa. The schematics showing the field oxide together with the UV resist mask can be seen in Fig.3.10 (8). In the next step (Fig.3.10 (9)) the field oxide in the mesa area is etched by BHF leaving only the mesa open and the rest of the wafer covered in the field oxide.

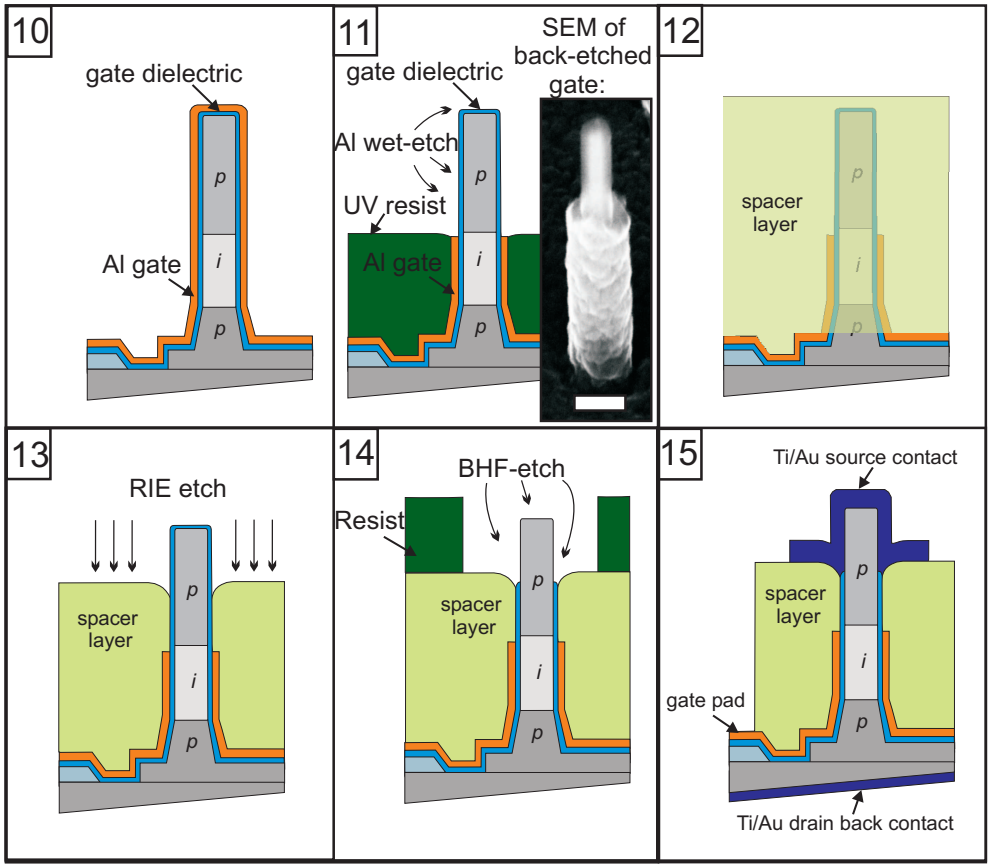


Figure 3.12: Schematic of process flow for vertical Si devices - gate alignment, spacer layer and top source contact. **(10)** & **(11)** Gate length definition: After depositing the gate dielectric and sputtering Aluminium for the gate metal the wafer is covered in UV resist and etched down in an RIE system with O_2 plasma to a desired height. An aluminium etch solution is used to etch the top metal away, leaving only the gate dielectric. The SEM inset shows a nanowire where the gate length is already defined. Scale bar is 100 nm. **(12)** Polyimide or BCB is then spin coated to cover the entire surface and nanowire. The polymer serves as the spacer layer between the gate and top source contact. **(13)** The height of the polymers is controlled by a RIE O_2 or O_2/SF_6 (for the BCB) plasma etch. **(14)** The top source contact is then defined by photolithography. A BHF dip is done to remove the gate dielectric in the top nanowire, followed by metallization and lift-off. To access the gate pads for measurements the polyimide or BCB is etched away over the gate pads by a RIE etch. **(15)** The finished device with the top source contact, the drain contact on the back of the wafer and gate.

Gate Stack

For the gate dielectric 15 nm of PECVD oxide is deposited and subsequently the sample is loaded into a sputtering tool to deposit 100 nm of Aluminium for the gate metal (Fig.3.12 (10)). To define the vertical gate length UV resist is spun on the wafer and etched down to a desired height of the nanowire length. A critical part is to get the correct height of the resist in

accordance with the height of the intrinsic region of the nanowire. The Aluminium on the top part is wet-etched using a custom etch solution (85 vol % phosphoric acid, 5 vol % nitric acid and 10 vol % H_2O). Fig.3.12 (11) shows the schematics after the Aluminium etch and a SEM image of a single nanowire where the gate length is already defined and the resist stripped.

Contacts to the Nanowire

The doped top part of the nanowire is used as the source contact in this architecture. For this, a spacer layer is utilized to isolate the gate from the top part. The spacer layer should exhibit a low dielectric constant to minimize capacitive coupling between the source and gate. Good isolating polymers with low dielectric constants utilized here are polyimide ($\epsilon \approx 3.5$) and a bisbenzocyclobutene-based (BCB) polymer ($\epsilon \approx 2.5$). Either polyimide or BCB is spin coated, baked and then back etched with a O_2 or O_2/SF_6 reactive ion etch, respectively. The top contact is then defined by photolithography and evaporation of 25 nm Ti and 100 nm Au. The backside of the wafer serves as the drain contact and is metallized as well. To access the gate pads for measurements later on the polyimide or BCB is again etched away over the gate pads by a reactive ion etch. The schematics of a finished device can be seen in Fig.3.12 (15).

PROCESS ISSUES

This section explores the process issues which arise during fabrication of vertical devices. Bottlenecks which imply an adaptation of the process flow are addressed. Solutions are investigated and an improved process will be shown.

Catalytic Etching of Si by Au Residues

One issue concerning VLS-growth with Au seed particles are Au residues remaining on the surface of the Si nanowire after the growth process. This poses a challenge for further processing of the Si nanowires since Au can catalyse a series of chemical reactions of silicon with wet chemicals, dry process gases, or even ambient atmosphere [RELD07]. Although the seed particle is removed in KI/I_2 solution immediately after growth, Au residues remain. The catalytic etching of the Si nanowire becomes apparent when longer etching in BHF is done, for example when the isolation oxide is removed after implantation or drive-in (see Fig.3.10). The chemical reaction governing the catalytic etching in HF solution can be written as:

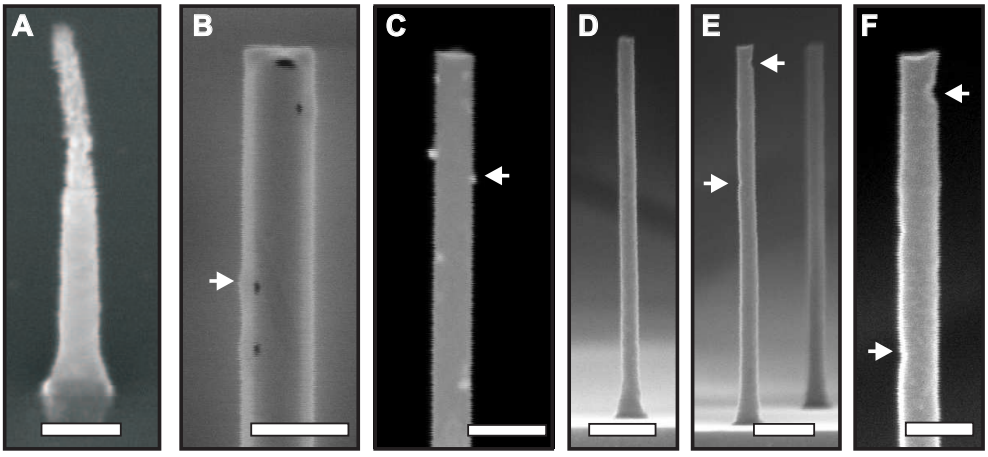


Figure 3.13: SEM images of Si nanowires epitaxially grown on Si<111> substrate. **(A)** A Si nanowire after implantation and removal of isolation oxide showing the top part etched. **(B)** Si nanowire thermally oxidized after BHF and KI/I_2 treatment. Below the 10-nm-thick oxide, agglomerated Au clusters can be seen. **(C)** the same Si nanowire as in **(B)** but with the oxide stripped, showing Au clusters left on the surface. **(D)** Si nanowire after second BHF-KI/I_2 etch exhibiting a clean, smooth surface. **(E)** and **(F)** The presence of larger Au clusters during 800°C oxidation results in a pitting of the nanowire surface. Scale bars are 100 nm, except for (D) and (E), which are 200 nm.

$$Si + 4HF_2^- + h^+ \quad \rightharpoonup \quad SiF_6^{2-} + 2HF + H_2 + e^- \tag{3.1}$$

The strong polarization in HF weakens the Si backbonds on the surface. The presence of both HF and H_2O then breaks these bonds and the Si is removed. Fig.3.13 A depicts a nanowire after the isolation oxide has been removed in BHF (7:1) solution for about a minute. It shows that the top part of the nanowire which is exposed much longer to BHF is etched almost completely away. This is unexpected because the etch selectivity of SiO_2 to Si is very high in BHF solutions. Thus, the Si nanowire should not be etched at all after being immersed in BHF. This finding points towards a catalytic etching effect of Si in BHF [BLG+09]. To investigate this catalytic etching of Si, test substrates with undoped nanowires are cleaned with the BHF – KI/I_2 procedure which removes Au seeds and residues from the surface of the Si nanowires. To check whether Au residues still remain, the wafer is heated in an RTA. Since Au diffuses very quickly in Si, Au agglomerates should be visible after a thermal treatment. This is indeed the case as shown in Fig.3.13 B. A thermal anneal at 800°C for 10 min in the presence of oxygen is done which results in the formation of a 10-nm-thick thermal oxide around the Si nanowire. The dark spots seen on the wire in Fig.3.13 B were not present before the heat treatment and are identified as gold particles formed by agglomeration of remaining Au traces during the heating step of the processing. Removing the thermal oxide by means of a BHF dip leaves the particles behind on the surface of the Si nanowire as seen in Fig.3.13 C. Another exposure to KI/I_2 removes these particles as can be seen in Fig.3.13 D.

The Au trace amounts leading to the agglomeration could have different origins; trace amounts of gold can redeposit on the wire surfaces from the etch solution. Secondly, the Au residues were covered or alloyed with Si such that the first KI/I_2 procedure could not remove them, or thirdly, the Au was trapped in the bulk of the nanowires crystal and diffused to the surface during the high temperature process. It is known that at temperatures above 800°C Au diffuses out of Si mainly via the so-called kick-out mechanism, which leads to an increased gold concentration at the surface with respect to the bulk of the silicon crystal [BLG+09]. The kick-out diffusion mechanism has been proposed as a means of purification of Si crystals [JD66].

Consequently, Au residues formed on the sidewalls either during growth or because of a subsequent heat treatment leave their marks on the Si nanowire surface and can be detrimental to further processing. In Fig.3.13 E and F pitting in the Si nanowire surface at the positions where larger Au particles had formed during the 800°C anneal can be seen. The Au particles eat into the Si surface of the Si nanowire, even in the short time between thermal oxidation and

the second BHF – KI/I_2 etch step. Hence, fast processing is mandatory to minimize surface damage.

To elucidate the effects of different HF-based solutions on the Si etching, a further experiment

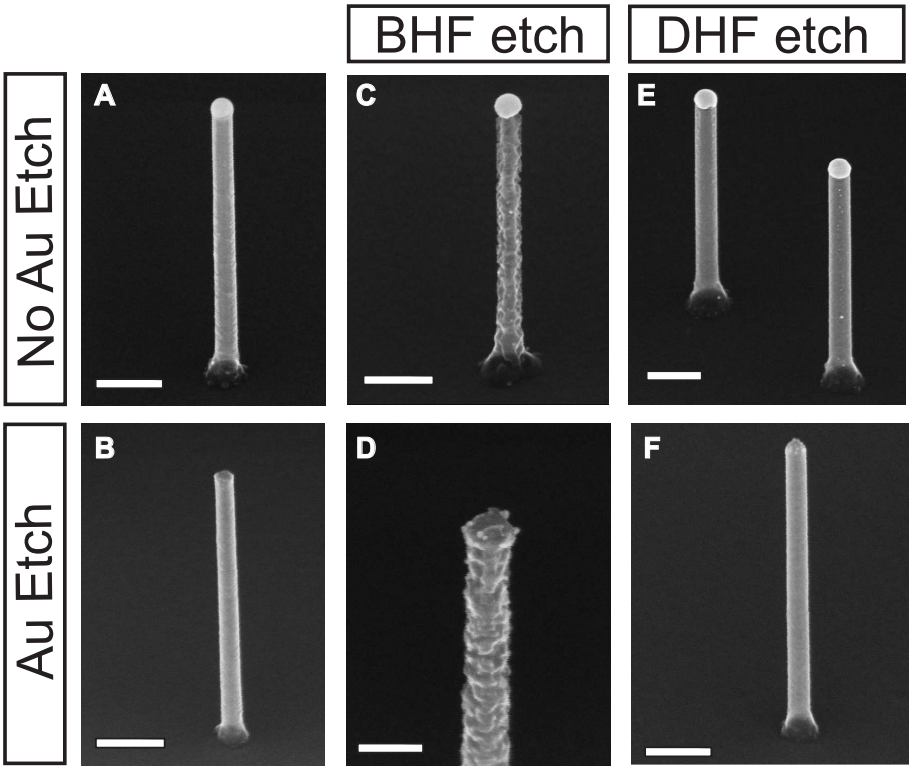


Figure 3.14: Si nanowires from one growth run treated with HF (5 minutes). **(A)** As-grown nanowire. **(B)** Nanowire after a BHF – KI/I_2 etch step removing the Au seed. **(C)** and **(D)** As-grown and Au-cleaned nanowires etched 5 min in BHF. **(E)** and **(F)** As-grown and Au-cleaned Si nanowires etched 5 min with DHF. BHF exposure can lead to surface damage while DHF leaves Si NWs undamaged. All scale bars are 200 nm, except in (D) which is 100 nm.

was done with BHF and diluted HF (DHF) solutions. The diluted HF solutions were 5% HF diluted in DI H_2O and all experiments were done at room temperature. Two sets of nanowires were used from the same nanowire growth run. Fig.3.14 A shows an as-grown Si nanowire and Fig.3.14 B depicts a nanowire from the same growth run but with the Au etched in KI/I_2.

In Fig.3.14 C and D an as-grown Si nanowire (C) and an Au-cleaned nanowire (D) are shown after being exposed to BHF for 5 minutes. Both exhibit etching of the Si nanowire, independent of whether the Au colloid was removed or not. The undoped nanowires here were grown on the same p-doped substrate but etched in different runs. The degree of surface damage varies from growth run to growth run, therefore only nanowires from the same growth run are used for the experiments. The Au-cleaned Si nanowires show the same degree of surface damage as

the as-grown ones. Similar results have been obtained also with other substrates (n, n^{++}, p, p^{++}), independent whether the BHF etch was performed in the dark or under illumination. Therefore, the Au residues do not seem to be solely responsible for the surface damage roughening during the BHF treatment. However, there is a big difference whether buffered HF or diluted HF is used for etching. No surface damage is observed when the Si NWs are exposed to DHF of nominally the same dilution as BHF. In Fig.3.14 E and F DHF exposed Si nanowires are shown with and without Au residues, respectively, with the same etching times as before. In contrast to BHF, DHF is not corroding the Si nanowires independent of Au residues or other processing parameters. The major difference between BHF and DHF is the *p*H of the solution. We have not yet established if this is the reason for the different selectivity.
It has to be noted that different nanowire growth runs exhibit different amounts of Au residue contamination due to variations in growth time. This makes it sometimes a less severe issue when etching in BHF. However, to circumvent BHF-induced roughening of the nanowire during processing a switch to only DHF seems to be the plausible solution. This is however marked by several limitations: When using UV resist as an etch mask, even highly diluted HF creeps along the interface of the resist and of the oxide covered nanowire. This leads to undesired etching along the entire nanowire. DHF is therefore not usable for mask-based etching.

Antenna Effect During Spacer Layer Etching

When etching the spacer layer in step 13, shown in Fig.3.12 (13), a uniform back-etch of the polyimide or BCB polymer is desirable across the entire substrate surface. A method to achieve this is to anisotropically etch the polymers vertically down in an RIE tool to the desired height. When etching down the polyimide or BCB the height has to be adjusted with respect to the gate. A large enough portion of the top nanowire has to be covered to avoid source-gate leakage. On the other hand, enough area of the top part of the nanowire has to stick out to ensure a large enough contact area at the top. During the reactive-ion etching the etch direction is vertical to the substrate and the anisotropy can be controlled by adjusting the applied voltage between the wafer holder and chamber electrode. For polyimide a pure O_2 plasma is used, for BCB a O_2/SF_6 plasma. Since the nanowires are conducting to the substrate and sticking out of the spacer layer during the etch, a high electric field builds up around them, similar to having a high electric field around an antenna. This high electric field attracts more charged ions

around the nanowire which leads to a higher etch-rate around the nanowires and thus, the formation of craters as seen in Fig.3.15 A in the case of BCB. This antenna effect has been seen for both BCB and polyimide and is independent of the doping concentration of the substrate. To study the possibility of reducing the craters the bias voltage as well as chamber pressure and power during reactive-ion etching were altered to etch more isotropically. A lower bias voltage and power together with higher chamber pressure leads to a more isotropic etch. This, however, has its limitations due to non-uniform height control of the spacer layer and the inability to start a plasma at very low voltages and high pressure, especially when using a pure O_2 plasma to etch polyimide. Varying the RIE parameters is therefore not a suitable method to control the polymer heights in a reproducible way.

A possible solution to prevent the etching of craters is a two-step process: This includes a first reactive-ion etch as seen in Fig.3.15 A, followed by spin-coating a thin film of diluted BCB (1:5 in T1100 rinsing solution) which fills the craters. A short reactive-ion etch then removes any residues on the surface of the nanowire sticking out. As a result, nanowires are sticking out of a nicely planarized surface with defined height as can be seen in Fig.3.15 B.

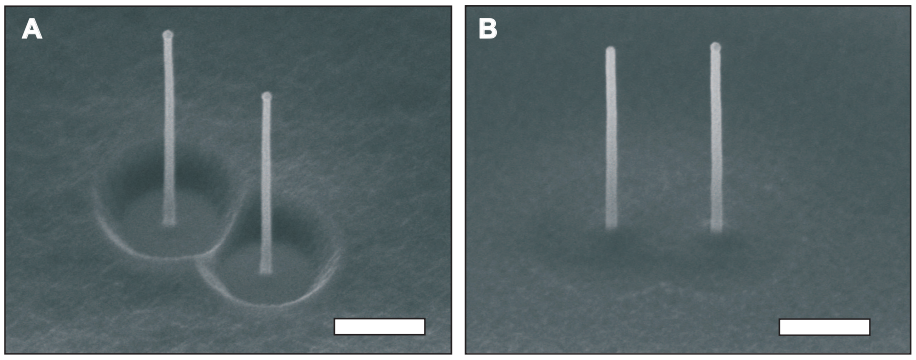


Figure 3.15: **(A)** Si nanowires after reactive-ion back-etching of BCB. Craters are seen around the nanowires due to an antenna effect. **(B)** After spin-coating the wafer in (A) with diluted BCB and a short rective-ion etch, the craters are filled up. Scale bars are both 200 nm.

Summary

The issues addressed here were solved by removing Au residues after growth and a two-step process to eliminate craters in the BCB spacer layer. Although Au residues were thought to be entirely removed from the nanowires with KI/I_2 some residues still remain which becomes

apparent when removing the isolation oxide in BHF in step 2 and step 5 of Fig.3.12. Even multiple process steps using KI/I_2 and a short BHF dip as explained earlier don't fully eliminate all Au residues. This is a limiting factor when using Si nanowires grown with Au seed particles.

FURTHER IMPROVEMENTS

Intrinsic MBE layer

There are limitations on the abruptness of the junctions when considering the vertical process introduced above. First, dopant diffusion from the substrate into the nanowire during growth can smear out the junction and second the doping at the top junction is not necessarily abrupt when using implantation or diffusion doping. Instead, abrupt junctions can be grown by MBE growth. Therefore, a 150 nm intrinsic Si layer, serving as the channel, is grown at a low temperature (500°C) MBE process to avoid dopant diffusion from the top of the doped Si substrate. The MBE layer is grown at IBM by Dr. Mirja Richter.

In-Situ Doped Nanowires

Following the MBE growth *in-situ* n-doped nanowires are grown on the top of the intrinsic MBE layer which again should lead to sharper interfaces, depicted in Fig.3.16 (1). Because higher doping densities as well as higher growth yield can be achieved by *in-situ* doping nanowires with Phosphorous. This approach is only considered for n-doped nanowires as p-doping causes tapering, as discussed before. *In-situ* doping also reduces the risk of catalytic etching of the Si nanowire when stripping the isolation oxide after implantation or drive-in as shown in Fig.3.10 (5) as long as oxide etching is avoided.
The schematics of the rest of the process flow are shown in Fig.3.16. The mesa etch step and vertical back-etch are interchanged in the new process, as the intrinsic segment first has to be defined along the nanowire (Fig.3.16 (2) and (3)).

Isolation Layers

After depositing the gate dielectric a BCB isolation layer is spin coated and back etched to the desired height. A second step where diluted BCB is spin coated and reactive-ion etched fills the craters around the nanowires (Fig.3.11 (4)).
All other steps remain the same as in the original process.

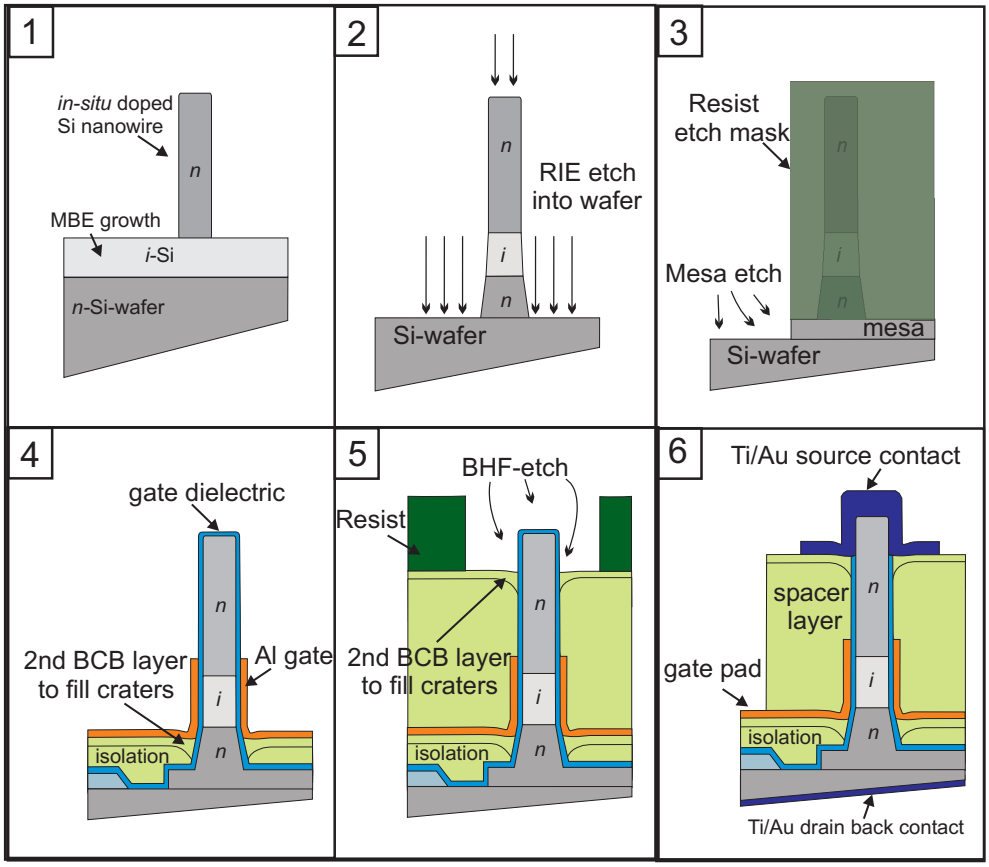


Figure 3.16: Schematic of improved process flow. **(1)** After a 150 nm thick intrinsic Si layer grown by low temperature MBE *in-situ* n-doped nanowires are grown leading to sharper interfaces at the wafer-MBE layer and nanowire-MBE layer. It also eliminates long exposures to BHF when removing the isolation oxide after implantation or drive-in. **(2)** Back-etch into the substrate. **(3)** Mesa etching. **(4)** Isolation layer and gate length definition: After depositing the gate dielectric a BCB isolation layer is spin coated and back etched to the desired height. A second step where diluted BCB is spin coated and reactive-ion etched fills the craters around the nanowires. After sputtering Aluminium for the gate metal the wafer is covered in UV resist and etched down in an RIE system with O_2 plasma to a desired height. An aluminium etch solution is used to etch the top metal away, leaving only the gate dielectric. **(5)** A BCB spacer layer is then deposited and the height is controlled by a RIE O_2/SF_6 plasma etch. A second diluted BCB layer is spin coated to fill the craters after the first RIE plasma etching. The top contact is then defined by photolithography, metallization and lift-off. **(6)** The finished device: After step (5) the gate pad is defined. The backside of the wafer serves as the drain contact and is metallized as well. To access the gate pads for measurements the BCB is etched away over the gate pads by a RIE etch.

3.3 Summary

In this chapter the developed process flows for lateral as well as vertical devices including issued and improvements was presented. The lateral process is versatile when it comes to utilizing different gate stacks. A new process for HfO_2 was developed with a gate-first approach to circumvent the low etch rate of HfO_2 in HF. The small differences in processing as compared to the process with the SiO_2 gate stack makes it a versatile tool to compare the two gate stacks while utilizing the same batch of grown nanowires.

The vertical process allows for a full wrap-gate architecture which improves the gate coupling on the channel. A full vertical process was developed for Si FETs. Issues arising during processing were discussed and solutions were provided. This included the reduction of BHF exposure to the Si nanowire to reduce catalytic etching due to Au residues. To reduce the formation of craters after etching back the BCB spacer layer, a second layer of highly diluted BCB was spin coated to fill the craters. To avoid smearing out at the bottom junction of the nanowire, a 150 nm thick intrinsic Si MBE layer was grown at a low temperature (500°C) MBE process to avoid diffusion from the top of the doped Si substrate. For the doping of the top part, instead of using implantation or diffusion doping, *in-situ* n-doped nanowires were grown on top of the intrinsic Si layer which makes the junction more abrupt. The vertical process can be adapted to several material systems with minor changes in the process flow. It is the basis for the integration of InAs on Si serving as single heterojunction tunnel FETs by our group [SMB+11].

4 Characterization of Si Based Devices

This chapter describes the experimental results on the electrical characterization of Si nanowire-based devices such as diodes, lateral Tunnel FETs and vertical FETs. Based on the fabrication scheme developed in the previous chapter the junction quality of *p-n* and *p-i-n* diodes is characterized and the influence of different gate stacks on Tunnel FETs is investigated in terms of current drive, substhreshold slope and temperature dependent behaviour. Furthermore, the experimental realization of vertical FETs is demonstrated for a nanowire with implanted top contact.

4.1 Lateral Tunnel FET

4.1.1 *p-n* and *p-i-n* Diodes

As explained in chapter 1 and 2, abrupt junctions are a prerequisite for good performance in Tunnel FETs. The more abrupt the junction profile which is characterized by the screening length λ (eq. 1.21, section 1.3), the higher the interband tunneling current becomes and thus, a higher on-current can be observed. An abrupt junction also leads to a steep inverse subthreshold slope *S*. It is therefore necessary to fabricate sharp junctions to improve device performance. A high source doping and control of doping levels is needed to effectively cut off the low (or high) energy portion of the source Fermi distribution. For our grown and *in-situ* doped Si nanowires high n-type doping has been achieved (see chapter 2), in particular n-type doping concentrations can be controlled from $1\times 10^{18}\text{cm}^{-3}$ to $1.5\times 10^{20}\text{cm}^{-3}$. To analyse the abruptness of *i-n* junctions of nanowires, TEM-based off-axis electron holography was

used to measure the i-n^+ junction [dHSC+09] which was carried out by Martien den Hertog at LETI. The junction abruptness was found to be between 7.5 nm and 30 nm per decade of carrier concentration. P-n and p-i-n nanowires where then used to fabricate p-n and gated p-i-n diodes for 2-point probe measurements. The p-n devices were fabricated by electron beam lithography, metallization and lift-off as described in chapter 3. The p-i-n devices were top-gated lateral Tunnel FETs whose fabrication process is also described in the chapter 3. The i-segment had a length of 500 nm which was presumably covered entirely by the gate which was left floating and the entire nanowire device was embedded in 20 nm PECVD SiO_2. The schematics of both devices as well as the I-V characterstics in a semi-logarithmic plot are shown in Fig.4.1. All devices were measured at ambient temperature. With the presence of series resistance, R_S, the forward current-voltage characteristics can be approximated by [Sze08]:

$$I_D = I_S\, e^{\frac{q(V_{DS}-I_D R_S)}{\eta kT}} \tag{4.1}$$

where I_D is the current, I_S the saturation current, V_{DS} the applied voltage and η the ideality factor. An ideal diode has an ideality factor of one. the ideality factor η at low bias can be obtained by fitting a straight line to the logarithmically plotted forward bias current and solving for η:

$$\eta = \frac{1}{2.3 \cdot slope \cdot kT/q} \tag{4.2}$$

A look at the rectification ratio measured at 1.5V, one finds a ratio of 233 and 4642 for the p-n and p-i-n diode, respectively. The current at 1.5V of the p-i-n diode is almost 2 orders of magnitude larger than that of the p-n diode. The ideality factor η which is around 2 for both devices, suggests that the forward bias is dominated by recombination in the space charge region. The ideality factor can also exceed 2 if contacts to the nanowire have a high contact resistance. In this case the metal-semiconductor contact acts as a reverse-biased Schottky contact. It has been shown that the ideality factor η is the sum of all η's of rectifying junctions and can be higher than 2 [SLGS03]. Values of 2 were reported for p-n Si and Ge nanowires [AVN+07], [TARG06]. The Schottky contact is likely stemming from the contact resistance on the p-doped part which has a lower doping density as explained in chapter 2. Four-point probe measurements on doped wire sections indicate that the n^+-contact is Ohmic, whereas the p-contact exhibits non-Ohmic behaviour. Thus, the p-doped part is not highly enough

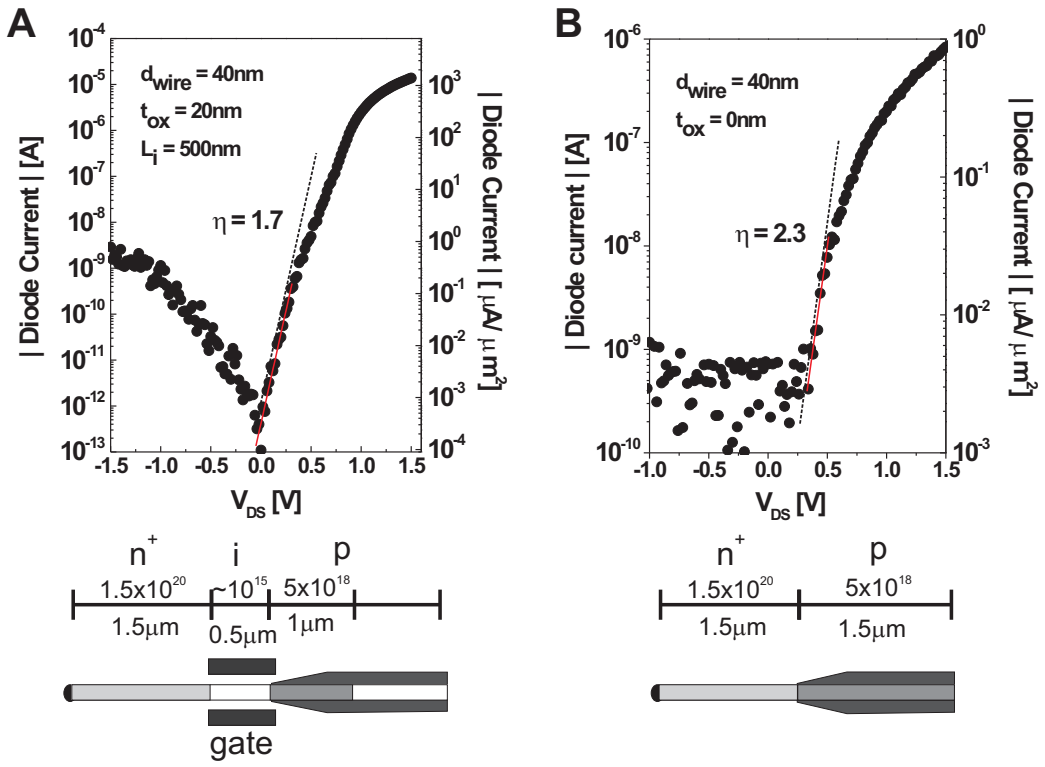


Figure 4.1: Electrical characteristics and schematics of a **(A)** Si *p-i-n* diode with floating gate and a **(B)** *p-n* diode. *I-V* characteristics were all measured at ambient.

doped which may lead to a Schottky barrier at the metal-p nanowire junction. In reverse bias the coated *p-i-n* diodes exhibit on average a lot less noise at low voltages than the blank *p-n* diodes. Although the n^+-doped part of the diodes is degenerate no tunneling and no NDR region is observed. This can be explained by the limited abruptness of the junction.

The *p-i-n* diode exhibits much larger currents in forward bias than the *p-n* diode. This is not obvious since one would assume that the "extra" intrinsic region in the *p-i-n* structure would lead to a higher series resistance and therefore lower currents in forward bias. The *p-i-n* diodes here give one of the lowest ideality factors reported for VLS-grown Si nanowires and show that the *i-n* junction indicate a well defined and good quality junction. Due to the floating gate on top of the intrinsic segment, the active profile in the segment is, however, not known. The workfunction of the gate metal could in principal shift the profile towards p-or n-type. In the next section the Tunnel FET operation of the *p-i-n* devices is investigated.

4.1.2 Tunnel FETs with a SiO_2 Gate Dielectric

In this section lateral Si nanowire Tunnel FET devices with SiO_2 gate dielectric are investigated. The devices studied have a 20 nm or 10 nm PECVD SiO_2 gate dielectric with Al gate. The gate length varies from L_G=600 nm to 800 nm to achieve full coverage of the intrinsic segment which has a length of L_i=500 nm. Top-gated devices are fabricated as explained in section 3.2.2. The devices are characterized electrically and performance factors such as drive currents, subthreshold slopes and I_{on}/I_{off} ratios are extracted.

The top-gate configuration allows almost a GAA control over the channel. The actual shape is, however, closer to a Ω-shaped gate. It is therefore assumed that the channel width is 75% of the nanowire perimeter. Thus, the effective width used for normalization is $W_{eff} = 0.75 \cdot \pi d$ as a function of nanowire diameter d. The effects of back gating have been investigated the previous work [HBS+07] of our group. The back gate is separated from the nanowire channel by the Si wafer and a 100nm thick thermal oxide. This leads to a less efficient gate control over the channel as has been reported. Consequently, in all electrical measurements, the substrate is grounded to reduce noise and not gated at all. As already pointed out in the fabrication section (section 3.2.2) the challenge during processing is to align the gate correctly over the source/channel region and at the same, to achieve an underlap at the channel/drain junction. Since this is not a self-aligned process there is always an uncertainty whether the gate is well aligned or not. With all measured devices it is easily observed when the tunnel junction (n^+-i) is not overlapped by the gate. In this case a diode characteristic but no gating effect is observed. The output characteristics of a device with a 20 nm SiO_2 gate dielectric and 600 nm gate length is shown in Fig. 4.2 A. The nanowire diameter at the n^+-i region is 40 nm. An I_{on} up to 0.5 μA/μm at a gate voltage of V_{GS}=-3 V is observed. The low-bias I_{on} (V_{GS}=-1V, V_{DS}=1 V) is about 0.014 μA/μm. Furthermore, the I_{on}/I_{off} ratio measured is around 6 orders of magnitude. A large threshold voltage, V_T, shift with V_{DS} bias is observed as illustrated in Fig.4.2 B. Here, V_T is defined as the V_{GS} at which I_D=1 pA. The slope has a value of 1.457 V/V. It has to be noted that the workfunction of the gate is not optimized here and the V_T shift could be partly due to the difficulty in aligning the gate position above the i-segment, as explained before.

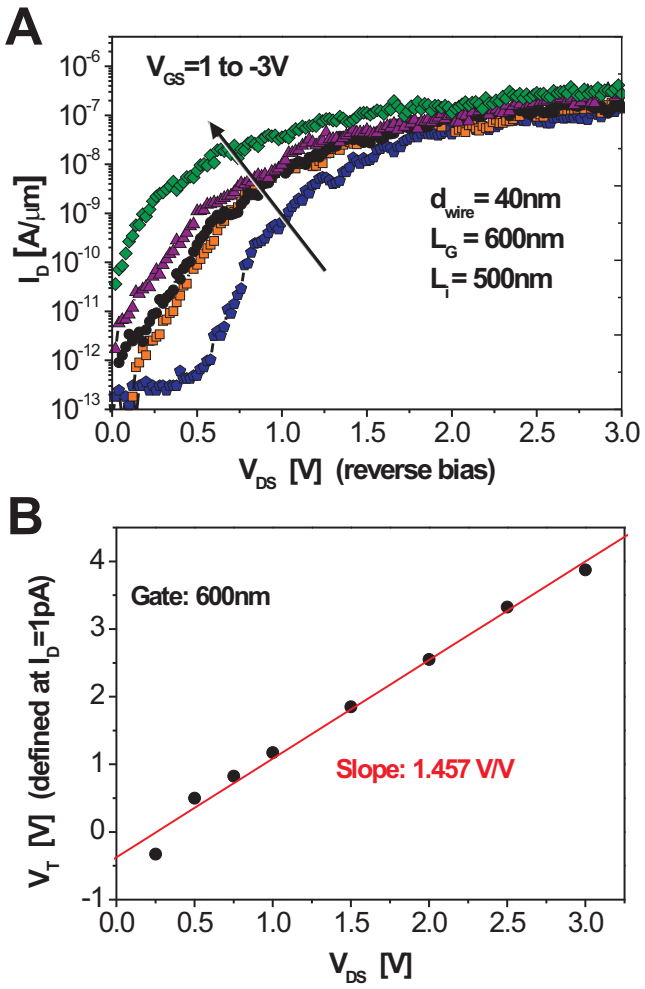


Figure 4.2: **(A)** Output characteristics of a Si NW TFET with the following parameters L_G=600 nm, L_i=500 nm, t_{ox}=20 nm, and d_{wire}=40 nm. The on-current reaches around 0.5 μA/μm. **(B)** Shift of the gate threshold voltage, V_T, with increasing V_{DS}. Here V_T is defined as the V_{GS} at which I_D=1 pA. The slope has a value of 1.457 V/V.

The transfer characteristics of the corresponding device are shown in a semi-logarithmic plot in Fig.4.3 A. Here a subthreshold slope in the range of 100 mV/dec can be observed over two to three decades of current at a V_{DS} of 0.5 V. An I_{on} of 0.3 μA/μm is achieved and I_{off} of $\approx$ 0.3 pA/μm, all measured under ambient. The devices are measured with a positive source (n^+) bias instead of a negative drain (p) bias. In the on-state the polarization shouldn't matter and it is mainly a means of notation. A close-up of the characteristic in the range between 0 and 1.6 V can be seen in Fig.4.3 B. For very small V_{GS} and over 1 order of magnitude the point-slope reaches values of almost 60 mV/dec.

Next, a device with a 800 nm long gate is studied. The overlap of both the tunnel junction

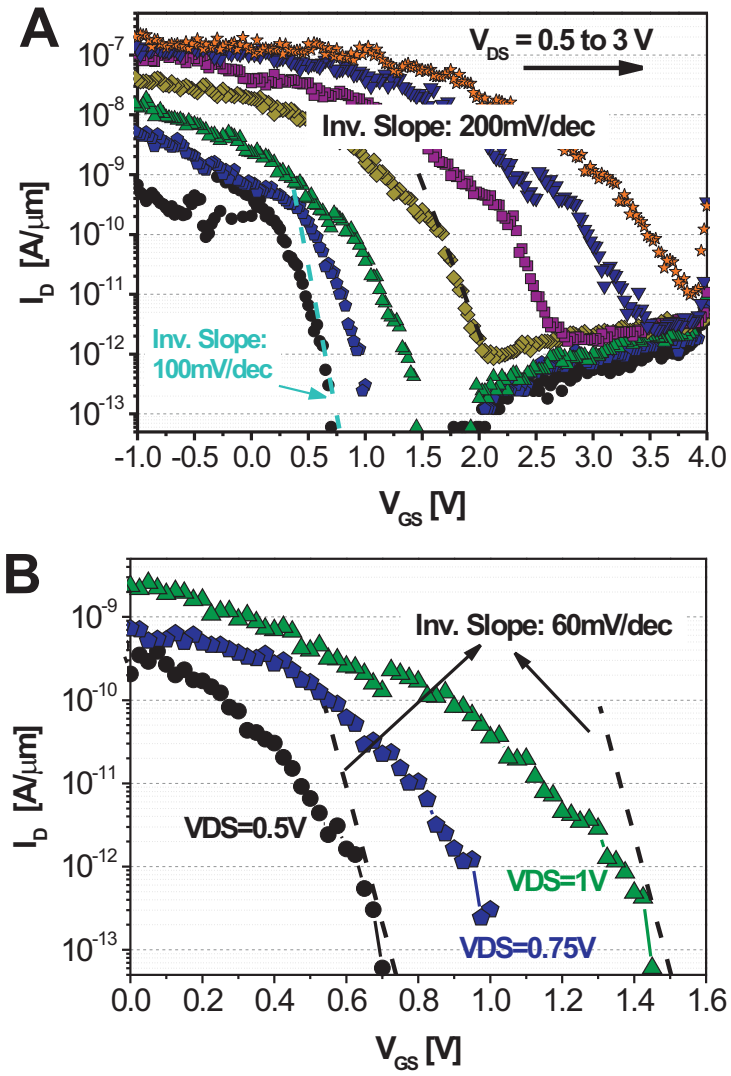


Figure 4.3: **(A)** Transfer characteristics of the TFET, with the p-i-n^+ diode reverse biased. L_G=600 nm, L_i=500 nm, t_{ox}=20 nm, and d_{wire}=40 nm. The dashed lines corresponds to a S of 100 mV/dec and 200 mV/dec, respectively. **(B)** Close-up of **(A)** for low V_{GS} bias revealing point-slopes of about 60 mV/dec. The device has an Al gate and the the source drain contacts are Ti/Au.

(n^+-i) and drain-channel junction(p-i) increases. The output characteristics are depicted in Fig.4.4. The I_{on} reaches up to 0.2 μA/μm at a gate voltage of V_{GD}=-4 V which is similar to the device before. A maximum I_{on} of 0.4 μA/μm is achieved and the I_{on}/I_{off} ratio measured is around 6 orders of magnitude like the device presented beforehand. The threshold voltage shift with V_{DS} bias is however smaller at a value of 0.924 V/V. The transfer characteristics

show an average subthreshold slope of 350 mV/dec over 4 orders of magnitude (Fig.4.5) and a low-bias subthreshold slope of 100 mV/dec. Although the device with the 800 nm long gate exhibits poorer device performance than the one with a 600 nm long gate, it is not evident whether the gate length plays a role. The important factor is the gate overlap on the tunneling junction and could be different for both devices. The large threshold voltage shift with V_{DS} bias indicates that there is a gate underlap at the tunneling junction. This leads to a tunneling width at the n^+-i junction which changes with changing V_{DS} bias. Consequently, The threshold voltage as well as the inverse subthreshold slope shifts with changing V_{DS} bias.

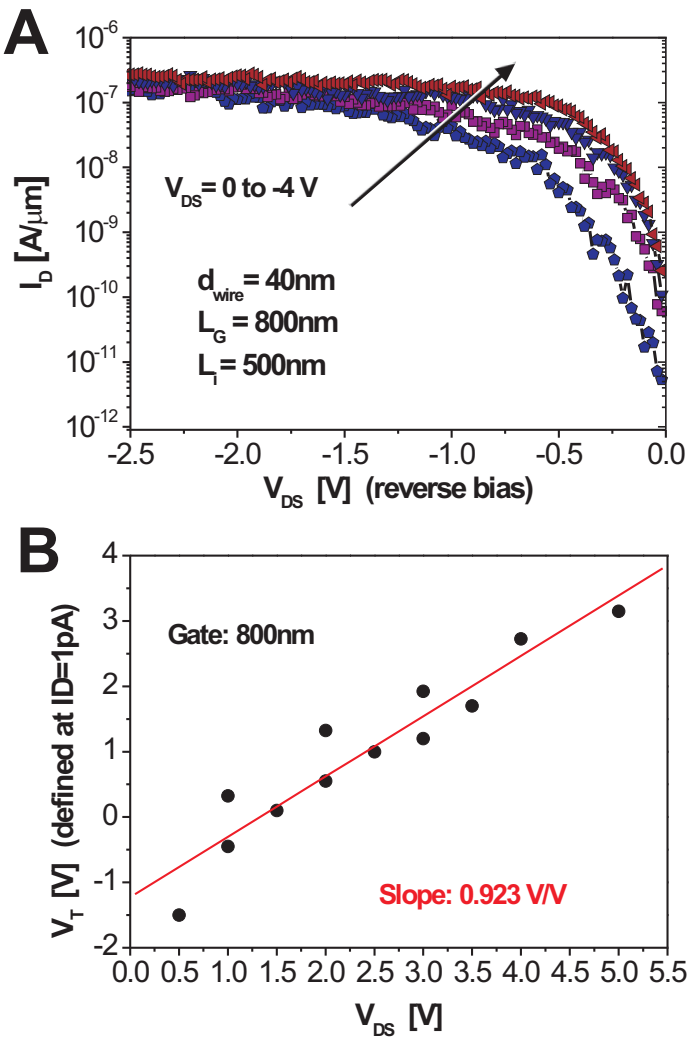


Figure 4.4: **(A)** Output characteristics of a Si NW TFET with the following parameters L_G=800 nm, L_i=50 0nm, t_{ox}=20 nm, and d_{wire}=40 nm. The on-current reaches around 0.2 μA/μm. **(B)** Shift of the gate threshold voltage, V_T, with increasing V_{DS}. The slope has a value of 0.923 V/V.

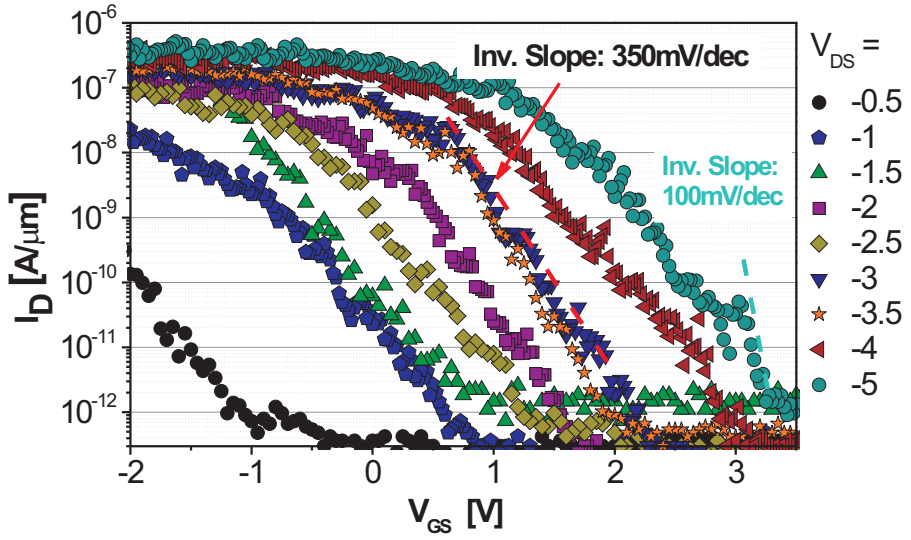


Figure 4.5: **(A)** Transfer characteristics of the TFET, with the p-i-n^+ diode reverse biased. L_G=800nm, L_i=500 nm, t_{ox}=20 nm, and d_{wire}=40 nm. The dashed lines corresponds to a S of 350 mV/dec. For low V_{GS} bias point-slopes of about 100 mV/dec are reached.

4.1.3 Tunnel FET Performance-Dependence on Gate Stack

As discussed in chapter 1 there is a variety of boosters in Tunnel FETs to improve performance. Apart from the material, optimized source doping, sharper tunnel junction profile, scaling to the quantum capacitance limit by thinning down the body and proper gate alignment, the use of a high-κ gate dielectric can improve the device performance substantially. The reduced effective oxide thickness (EOT) provided by these dielectrics can significantly improve the on-current, as discussed in the Introduction chapter. As explained in chapter 1 a device with a small screening length can therefore be scaled down further and at the same time maintain better gate control over the channel. λ is much lower for high-κ dielectrics at a given oxide thickness. For device performance, a lower λ value leads to an increased tunnel probability and lower inverse subthreshold slopes by improved gate coupling (see chapter 1). To reduce the EOT and thus increase gate coupling, devices with 5 nm HfO_2 were fabricated as explained in chapter 3 section. The nanowires were grown in the same batch as the samples with the 20 nm SiO_2 gate dielectric, presented in section 4.1.2. The wire diameter of the two devices is very similar with 40 nm for the tunnel FET with SiO_2 gate dielectric and 50nm for the tunnel FET with HfO_2 gate dielectric. The variation in nanowire diameters comes from variations in Au colloid size.

The impact of the smaller oxide thickness can be seen when calculating the screening length for both gate dielectrics using equation 1.12:

- 20 nm SiO_2, 40 nm nanowire, assuming κ = 3.9: λ=**39.5 nm**
- 5 nm HfO_2, 50 nm nanowire, assuming κ = 25: λ=**13.5 nm**

The HfO_2 sample should therefore exhibit better S values and higher drive currents due to the smaller λ and hence the higher transmission probability at the source-channel interface. Both devices are measured at room temperature. The HfO_2 sample is measured in vacuum, whereas the SiO_2 sample is measured under ambient conditions, thus the characteristics for the SiO_2 sample are more noisy which can be systematically observed on several devices measured at ambient. This does not however, influence the extracted device parameters.

The output characteristics of the tunnel FET with HfO_2 gate dielectric are shown in Fig.4.6 and exhibit the same order of magnitude in on-current as the SiO_2 sample, but a clearer dependence on V_{GS}. This could stem from the different alignment of the gate to the channel.

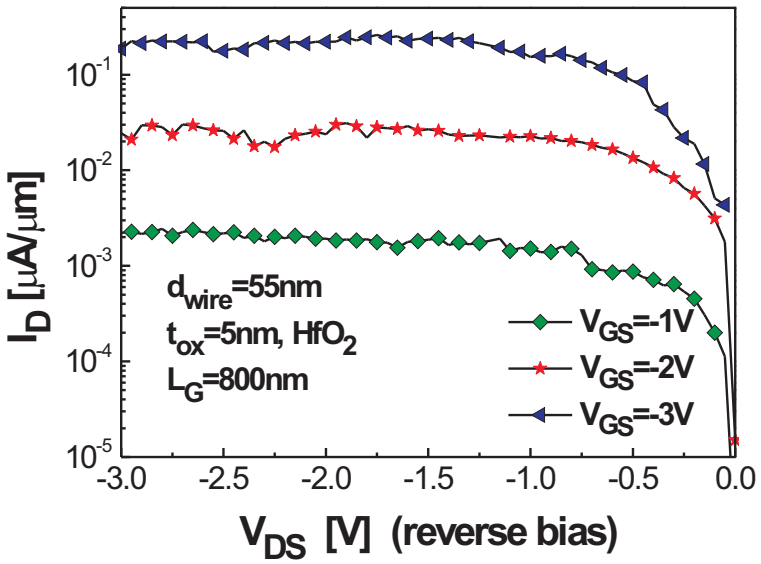


Figure 4.6: $I_D(V_{DS})$ characteristics for a Tunnel FET with HfO_2 gate dielectric, shown at V_{GS} values of -1V, -2V and -3V. The gate length here is 800nm and the metal used was Ti/Au.

The $I_D(V_{GS})$ characteristics of two different gate stacks, one TFET device with 20 nm SiO_2 gate dielectric and the same device as above with 5 nm HfO_2 gate dielectric, are shown in

Fig4.7. To facilitate the comparison of both devices the characteristics have been shifted so that they approximately posses the same threshold voltage. In the case of the Tunnel FET

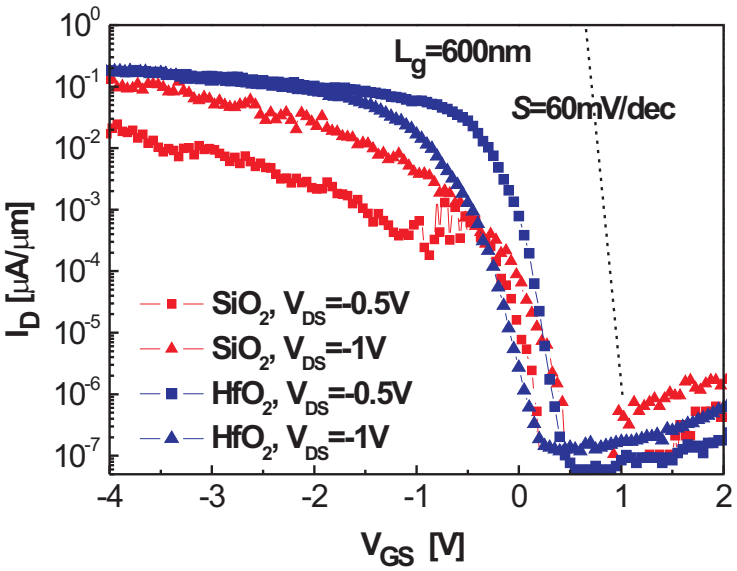


Figure 4.7: $I_D(V_{GS})$ characteristics for a TFET for two different dielectrics and V_{DS} bias. The diameter for the SiO_2 sample is 40 nm and the device is measured in ambient. The diameter for the HfO_2 sample is 50 nm and the device is measured in vacuum. This figure has been corrected for the difference in polarity and threshold voltage between the devices. The dashed line corresponds to a S of 60 mV/dec.

sample with SiO_2 as gate dielectric, I_{on} depends sensitively on the value of V_{DS}, and a greater difference between the characteristics for -0.5 and -1 V is observed. The I_{on} at $|V_{GS}|$ =2V and $|V_{DS}|$ =1V bias is 0.102 μA/μm for the HfO_2 sample, compared to only 0.024 μA/μm for the SiO_2 sample. At $|V_{DS}|$ = 0.5 V this difference is further increased to 0.084 μA/μm and 0.003 μA/μm respectively. The local minimum value of S is lower for the SiO_2 sample (≈60 mV/dec. compared to ≈90 mV/dec.), but this is mainly a result of the lower I_{off}. The device with HfO_2 as gate dielectric shows a higher I_{off} due to increased leakage through the HfO_2.

The average S measured between 10^{-7} μA/μm and 10^{-3} μA/μm is 120 mV/dec for the HfO_2 sample compared to 200 mV/dec for the SiO_2, which originates from the smaller screening length λ. The inverse subthreshold slope as a function of I_D is plotted in Fig.4.8 for both devices. As discussed in chapter 1 the inverse subthreshold slope of a Tunnel FET is no longer a constant in the subthreshold region, and as it is shown in Fig4.8 S is found to vary over the regions of operation. This, however, not only makes it difficult to compare individual devices

with one another and with literature.

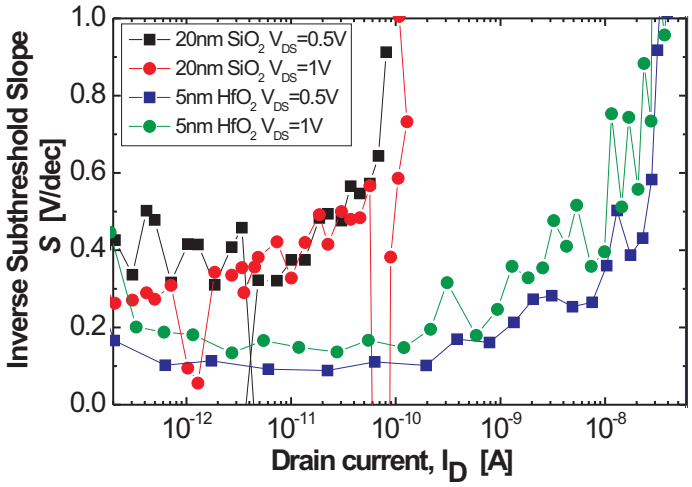


Figure 4.8: Subthreshold Slope S as function of I_D: Comparison between a Tunnel FET with 20 nm SiO_2 gate dielectric and Tunnel FET with 5 nm HfO_2 gate dielectric. The S value of the Tunnel FET with 20 nm SiO_2 gate dielectric varies strongly with I_D, compared to theunnel FET with 5 nm HfO_2 gate dielectric.

The use of a high-k dielectric is seen to improve performance in terms of both I_{on} (0.3 μA/μm) and average S, whereas the minimum point slope suffers due to increased leakage at low gate bias. Additional improvements can be made by enhancing the quality of the HfO_2 layer which can be achieved by reducing leakage and interface state densities. The issue of the leakiness of HfO_2 was further investigated by capacitance measurements and it was found that a higher deposition temperature of HfO_2 decreased the leakage. This, however, would make the HfO_2 layer on top of the nanowires impossible to remove and would require a different process than the one described in section 3.2.2.

Low-Temperature Characteristics

Temperature-dependent measurements provide additional information to discriminate pure tunneling current from thermionic emission. A Tunnel FET, as discussed also in the chapter 1, possesses a temperature-dependency different from that of a MOSFET. Temperature dependent measurements is one characteristic to identify a pure Tunnel FET and discriminate it from field-induced tunneling through a barrier in a MOSFET-like structure. Low temperature measurements were done in a flow cryostat setup for both gate stacks discussed in the

previous section . Tunnel FETs with a 10 nm SiO_2 gate dielectric were studied. These devices should exhibit the same temperature dependence as the equivalent sample with a 20 nm SiO_2 dielectric from the previous section. The nanowires again were taken all from the same growth batch. The same devices with 5 nm HfO_2 gate dielectric as in the previous section were used for temperature dependent measurements.

To evaluate the temperature dependence of the devices, an Arrhenius plot is made where

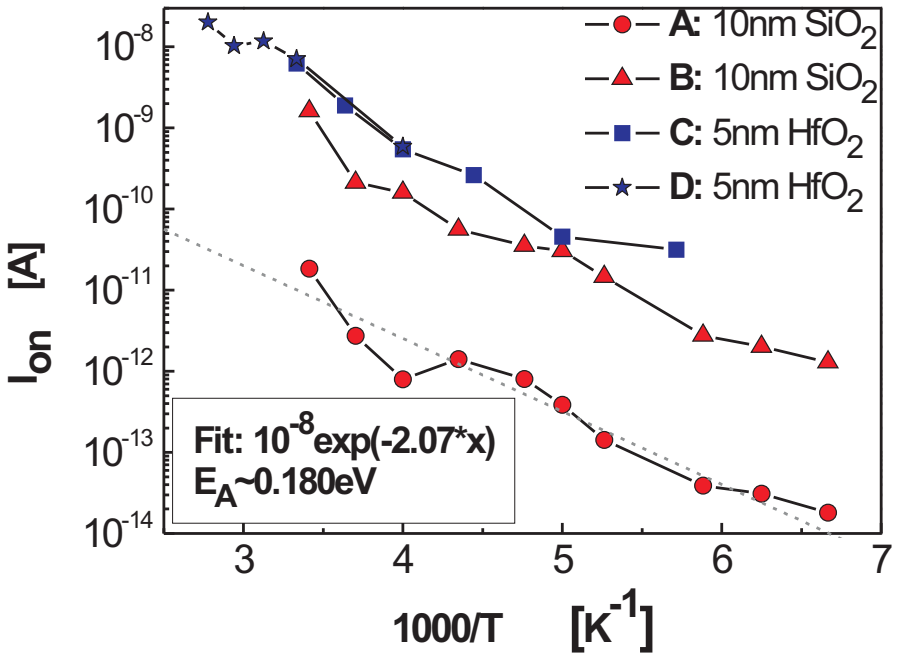


Figure 4.9: Arrhenius plot of I_{on} for different Tunnel FET devices and operating conditions. **A**: 10nm SiO_2 gate dielectric. V_{DS} = -0.5 V, V_{DS} = -1 V. **B**: Same device as in **A**. V_{DS} = -1 V, V_{DS} = -2V. **C**: 5 nm HfO_2 gate dielectric. V_{DS} = -0.5 V, V_{DS} = -1 V. **D**: Different 5 nm HfO_2 sample. V_{DS} = -0.5 V, V_{DS} = -2 V. The dashed line corresponds to $10^{-8}\exp(2.07 \cdot x)$.

a specific I_{on} of various Tunnel FETs with both HfO_2 and SiO_2 gate dielectric is measured at different temperatures and then plotted against the inverse temperature. A clear trend of exponentially increasing on-current with increasing temperature is seen in Fig.4.9.Both curves seem to follow a the same trend corresponding to an average activation energy of 0.180eV. This behaviour is similar to the temperature-dependence of a Schottky barrier governed by thermionic emission [AAMW03]. If I_{on} would be limited by tunneling a much weaker temperature dependence is expected due to the small temperature dependence of the band gap [BSE05]. Therefore the behavior of the I_{on} of the nanowire Tunnel FET seems to be lim-

ited by a potential barrier. Later studies of our group showed that by improving the contact metallization on the p-side with Ni/Au instead of Ti/Au as well as annealing the contacts, the criteria for which a Tunnel FET can be distinguished from a MOSFET such as a distinct low-temperature behavior, was observed [MBS+11]. Thus, the barrier was removed when a Ni/Au contact metallization was used.

In summary, HfO_2 and SiO_2 as gate dielectric on Si nanowire Tunnel FETs was compared from the same batch of VLS-grown nanowires. Superior device performance is owed to the device with a HfO_2 gate stack due to a lower screening length. Due to a stronger gate coupling the tunnel FET with HfO_2 gate dielectric exhibited the highest I_{on} of 0.1 μA/μm and the steepest average S of 120 mV/dec, combined with an I_{on}/I_{off} ratio on the order of 10^6. Temperature dependent measurements showed a nonideal temperature behavior, which was due to a potential barrier at the p-type region caused by the Ti/Au contact. This potential barrier may well have limited the I_{on} of the Tunnel FETs. It is anticipated that it will be possible to improve the performance of Tunnel FETs even further. In the future, a reduction of the NW diameter and a further decrease of the electrical oxide thickness should boost the I_{on} even further in all Si nanowire Tunnel FETs.

4.2 Vertical FET

The following section gives an overview on vertical FETs which were fabricated by the process introduced in chapter 3. The vertical process is also adaptable to the ongoing development of vertical InAs on Si TFETs and can be easily adapted to vertically etched nanowires; hence, the results here serve as a proof of concept for the vertical geometry. A p-i-p structure serving as a pMOSFET is presented here. Due the the limitations during processing, it was not possible to fabricate nMOSFET with Phosphorous diffusion doped top contact. The vertical Si pMOSFETs have a Boron-implanted top contact and a 15 nm SiO_2 gate dielectric with a 550 nm long Al gate as seen in a schematic in Fig.4.10 A. The top contact is 10 nm Ti and 80 nm Au. The transfer characteristics of 2 devices are shown in Fig.4.10 B. The two devices have almost equal I_{on} which is in the order of 0.9 nA/μm. The low on-current is not limited by the implantation but rather by the interface of the top contact as well as the short contact length. The inverse subthreshold slope S is 250 mV/dec for both devices. They, however, differ in threshold voltage. The high S value originates from the quality of the PECVD gate oxide with the average value being between 200 and 250 mV/dec. This is also found for other lateral FETs with PECVD gate oxide fabricated in our group. The characteristics are generally a proof of concept for the vertical design and device fabrication and are not used for benchmarking against lateral Tunnel FET devices.

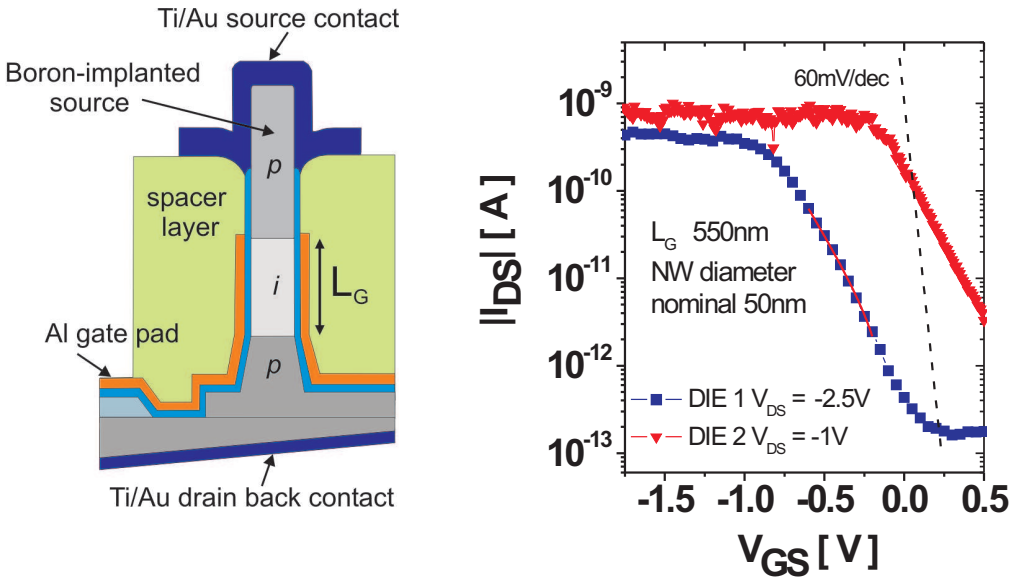


Figure 4.10: **(A)** Schematic of a fabricated vertical pMOSFET with Boron-implanted top part. Transfer characteristics of 2 vertical Si pMOSFETs with 15 nm SiO_2 gate dielectric and a 550 nm long Al gate. Dashed line corresponds to 60 mV/dec.

4.3 Summary

This chapter discussed the experimental work done on Si nanowires devices. It started out by describing the *I-V* characteristics of diodes with in-situ *p-n* and *p-i-n* doping profiles were fabricated and electrically characterized. Devices showed good ideality factors $\eta \approx 2$.
P-channel Tunnel FETs based with the same in-situ *p-i-n* doping profile as before were fabricated and electrically characterized. Two different gate stacks, namely 20 nm SiO_2 and 5 nm HfO_2 were investigated and revealed the benefits of high-κ dielectrics for Tunnel FETs. The device having the strongest gate coupling (5-nm HfO_2) exhibited the highest I_{on} of 0.1 μAμm and the steepest average $S \approx 120$ mV/dec, combined with an I_{on}/I_{off} ratio on the order of 10^6. Temperature-dependent measurements were carried out, showing a non-ideal temperature behaviour, and it was demonstrated by later studies of our group that this was due to a potential barrier at the p-type segment caused by the Ti/Au contact. The barrier was removed when a Ni/Au contact metallization was used. This potential barrier may well have limited the I_{on} of the Tunnel FETs.
Vertical Si pMOSFETs with a Boron-implanted top contact and a 15 nm SiO_2 gate dielectric were fabricated as a proof of concept for the vertical design and device fabrication. The inverse subthreshold slope *S* was measured to be 250 mV/dec for each device and a low on-current of 0.9 nA/μm.

5 Doping of InAs Nanowires and Realization of Tunnel Diodes

The shift from all-Si Tunnel FETs to heterostrucutre Tunnel FETs based on III-V material has the goal to improve the band-to-band tunneling (BTBT) rate by an optimized band alignment, a low effective bandgap and a low effecitve mass which III-V semiconductors, for example InAs and InSb, have. As discussed in the Introduction chapter there have been first experimental realizations for III-V homojunction Tunnel FETs based on InGaAs [ZCW+10] [MMK+09] as well as staggered InGaAs/InP heterojunction Tunnel FETs with tunneling occuring normal to the gate [ZLL+11] [ZLL+12]. First heterojunction Tunnel FETs based on InAs/Si were fabricated in our group [SMB+11] and by Tomioka *et al.* [TF11] by growing non-intentionally doped InAs nanowires on Si wafers. This has the advantage that channel, drain and carrier wafer material is Si and InAs is only used as a low bandgap source. The use of an InAs source is promising due to the electrical properties mentioned previously. In the case of the InAs on Si nanowire Tunnel FET higher n-type doping levels in the InAs source should improve the on-current substantially [SMB+11]. It is therefore necessary to control the doping concentration in the InAs nanowires which is presented in the first part of the chapter. It marks the first step towards device performance improvements for InAs-Si heterojunction Tunnel FETs and starts off by investigating n-type dopant incorporation in InAs nanowires, its effect on nanowire morhphology and electrical characteristics. Different doping species such as Si, S, C, and Te are studied. A new method to establish doping densities and mobility using the Seebeck effect is introduced. Here, the measured resistivity is directly related to mobility and doping density. The goal is to establish accurate doping densities without the need of measuring mobility. Compensation effects can be seen at high Sulphur doping which might be related to Sulphur complexes within InAs. The effect of compensation is further studied by Seebeck measurement

and it is found that the presence of Sulphur complexes may substantially enhance the Seebeck coefficient. In the second section vertical nanowire tunnel diodes from InAs homojunctions are characterized by temperature dependent measurements.

5.1 Resistivity Measurements

When measuring nanoelectronic devices it is important to include the effect of the contact to the device on the acquired data. If the contact is not Ohmic, that is the contact doesn't have a negligible resistance compared to the channel material, the device is strongly influenced by the contact resistance. There are several methods to obtain Ohmic contacts depending on the type of material and application such as doping the contact region to lower the Schottky barrier between the contact metal and semiconductor, surface preparation or interface engineering to de-pin the Fermi level by inserting a thin interfacial layer [CFGH04] [GKR$^+$09], to name a few. In contrary to Si, InAs has a small bandgap (0.35 eV compared to 1.11 eV in Si) and the Fermi level is pinned into the conduction band leading to the formation of an accumulation layer at the interface [CHL89]. InAs therefore forms Ohmic contacts with most metals given that no native oxide is present on the InAs surface which gives rise to a potential barrier. A good way to check this is to compare 4-point and 2-point measurements. However, as will be shown below, to derive the exact contact resistance to InAs nanowires and nanowire resistivity several considerations have to taken into account. In order to avoid contact resistances 4-point probe measurements are conducted. The resistance of the actual nanowire material can thus be measured and the resistivity derived. Additionally, 2-point transmission line measurements are performed between the varying electrode spacings.

Fig. 5.1 shows 2-point transmission line and 4-point probe measurements from the same single InAs nanowire device. The resistance of each 2-point probe measurement is plotted against the spacing of the electrodes where the resistance is measured. The total resistance increases linearly with the nanowire length. The linear curve can be extrapolated to zero electrode spacing which reveals the value of twice the contact resistance. The total resistance of a wire can be described by the following equation:

$$R_T = 2R_C + \frac{\rho_S}{\pi r^2} l \tag{5.1}$$

where r and l are the wire radius and length, respectively, ρ_S the semiconductor resistivity

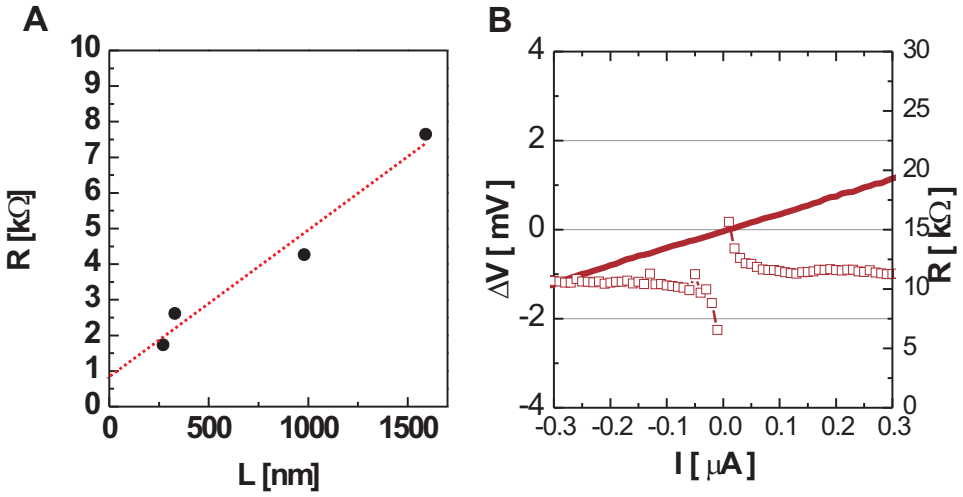


Figure 5.1: 2-point transmission line and 4-point probe measurements of the same InAs nanowire. **(A)** 2-point configuration: measured resistance as a function of electrode spacing showing a linear increase in resistance. **(B)** 4-point probe: voltage drop (solid line) measured between two inner electrodes and resistance (boxes + line) as a function of the current flowing between the two outer electrodes.

and R_C the contact resistance. A model by Mohney *et al.* [MWC+05] using Bergers general approach [Ber72] relates R_C to:

$$R_C = \frac{\rho_S L_T}{\pi r^2} \coth\left[\frac{L}{L_T}\right] \tag{5.2}$$

where L is the length of the contact and L_T the transfer length. The total resistance is then:

$$R_T = \frac{\rho_S}{\pi r^2}\left(2L_T \coth\left[\frac{L}{L_T}\right] + l\right) \tag{5.3}$$

The transfer length can be thought of as the distance over which most of the current transfers from the semiconductor into the metal or vice versa. If it is furthermore assumed that the metal contacts wrap around 75% of the wire circumference, the transfer length is

$$L_T = \sqrt{\frac{2r\rho_C}{3\rho_s}} \tag{5.4}$$

where ρ_C is the specific contact resistivity. The transfer length typically varies between 150 and 250 nm in both Si and InAs nanowires. Note that this model is only valid when the contact resistance is larger than the resistance of the wire segment under the contact. This is however not always the case as the following will show. In order to extract the exact contact resistivity

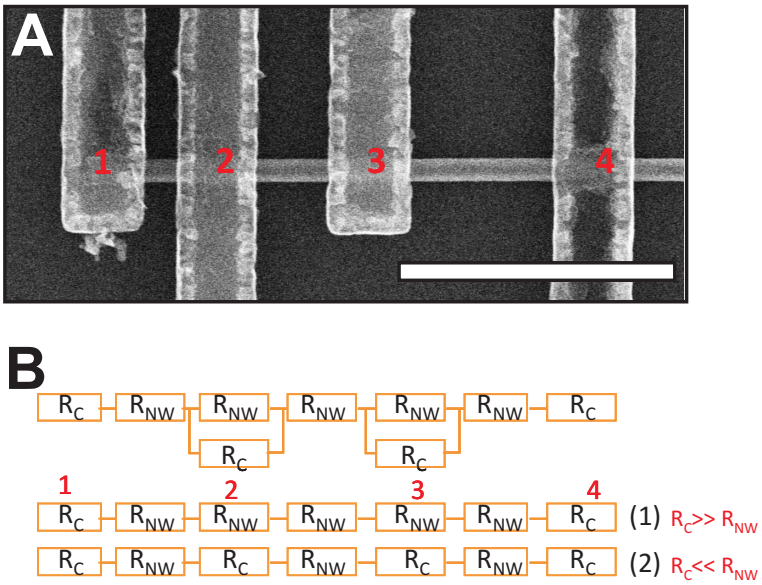


Figure 5.2: **(A)** SEM picture of single InAs nanowire device with 4 electrodes, scale bar is 1 μm. **(B)** Equivalent circuits for the device above: Actual circuit, circuit where contact resistance, R_C ≫nanowire resistance, R_{NW} and circuit where $R_C \ll R_{NW}$.

several assumptions have to be made. These assumptions can be best understood in an equivalent circuit. Shown in Fig. 5.2 is a SEM picture of a single InAs nanowire contacted by 4 electrodes, labelled from 1 to 4. 2-point transmission line measurements are done between all electrodes, i.e. 1-2, 1-3, 1-4, 2-3, 2-4 and 3-4, and the measured resistance is then plotted against the electrode spacing. The question arises whether to include the entire length between the electrodes in the plot or only the length in between the contact electrodes. The equivalent circuit of the device (Fig.5.2) incorporates all nanowire resistances in series to each other and all contact resistances to the nanowire since the current can flow through the metal contacts and/or through the nanowire. The 2 contact resistances in the middle are therefore in parallel to the fraction of the nanowire resistances. This circuit is valid if the resistance of the nanowire pieces under the contact are of the same order as twice the contact resistance (current travelling into the contact metal on one side and out of the metal on the other side). If, however, the contact resistance is much larger than the resistance of the nanowire piece under the contact, the contact resistance can be neglected when considering the length between the two electrodes measured ($R_C \gg R_{NW}$). The total length is therefore the entire length including the length under the nanowire. In this case equations 5.2 and 5.3 are not valid any more. In the other case when $R_C \ll R_{NW}$ the current travels preferably into the metal contact on one side and back into the nanowire at the other end. The length in the metal is negligible

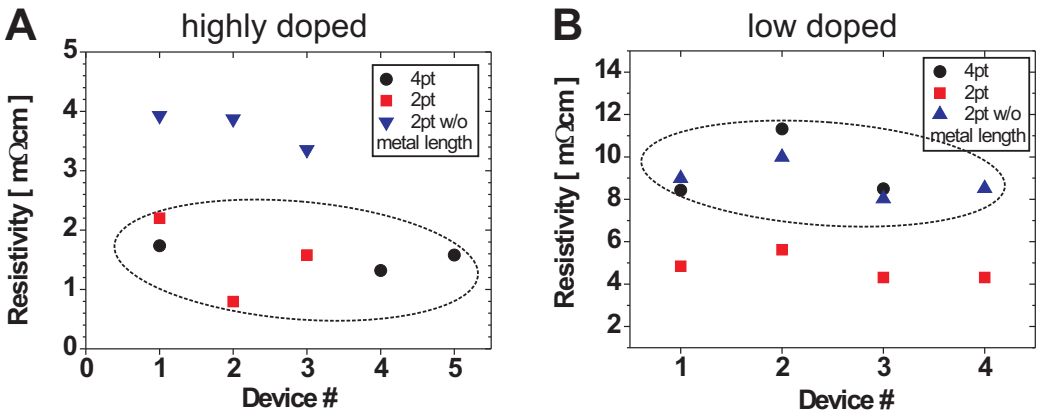


Figure 5.3: Resistivity of single InAs nanwoires derived by 4-point probe (black circles) and 2-point measurements, taking the full length between two electrodes into account for the analysis (red squares) and only the length in between electrodes without the length under the contact (blue triangles). **(A)** At low nanowire resistivity ($R_C \gg R_{NW}$) the 4-point resistivity coincides with the 2-point using the full length. **(B)** With nanowires having a higher resistivity ($R_C \ll R_{NW}$ the 4-point probe values coincide with the 2-point values where only the length between the electrodes is used for the analysis.

due to its much lower resistivity and thus only the length in between electrodes is counted to the total length. The two cases are shown in Fig.5.3 where 2 batches of nanowires were measured with different doping densities: Fig.5.3 A) displays the case where $R_C \ll R_{NW}$ and the current runs through the nanowire pieces under the electrode. Taking the full length into account the calculated resistivity coincides with the one derived from the 4-point probe measurement. At higher nanowire resistances ($R_C \gg R_{NW}$) the 2-point resistivity coincides with the 4-point probe when only taking the length in between the electrodes into account. These two simple cases have to be considered when extracting nanowire and contact resistivity to avoid misinterpretation of the data.

5.2 Doping Study

As covered in previous chapters the possibility to change both the charge-carrier type and density from insulator to near metal by adding dopants is an important factor to enhance device performance. *In-situ* doping is an effective method to achieve control over doping levels and in particular the junction abruptness in nanowires, which is especially important for tunnel diodes ([WPW+10], [BSB+11]) and Tunnel FETs ([SMB+11], [BKS+08]). For this reason, appropriate dopants are studied in the following section and chosen based on their

effect on morphology and maximum obtainable doping concentration. The doping densities are extracted by means of using three reference methods which are independent of mobility. The effect of compensation when doping with Sulphur is studied in more detail by Seebeck measurements showing that the presence of Sulphur complexes may substantially enhance the Seebeck coefficient.

5.2.1 Effect of *in-situ* Doping on Morphology

The addition of doping during nanowire growth often influences the axial, ⟨111⟩ and radial, ⟨1-10⟩, growth rates, resulting in non-homogeneous radial and axial doping profiles. It can also affect the morphology and nucleation. As pointed out before various dopant precursors (Si_2H_6, H_2S, DETe, CBr_4) are added during growth at different flow ratios $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$.

Doping with DETe

The addition of the slightest amount of DETe ($\Phi_{DETe}/(\Phi_{TMIn} + \Phi_{TBAs})$ 10^{-6}) completely inhibits ⟨111⟩ growth and only ⟨1-10⟩ growth is possible, making DETe non-suitable for in-situ doping of nanowires unless pure shell doping is needed.

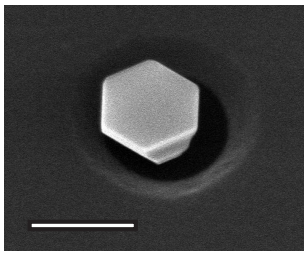


Figure 5.4: Addition of the slightest amount of DETe inhibits ⟨111⟩ growth, making ⟨1-10⟩ growth only possible. Scale bar is 200 nm.

Doping with CBr_4

It is observed that when using CBr_4 the nucleation of nanowires is drastically reduced at $\Phi_{CBr4}/(\Phi_{TMIn} + \Phi_{TBAs})$ ratios larger than 10^{-3}. As will be shown in the next section CBr_4 is not suitable for n-type doping.

Doping with H_2S

In contrast, doping of InAs nanowires with hydrogen sulfide (H_2S) shows no change in growth rates, morphology or nucleation as compared to undoped wires, even for $\Phi_{H2S}/(\Phi_{TMIn} + \Phi_{TBAs})$ ratios as large as 10^{-2}. Fig. 5.5 B displays a sulphur-doped wire, in which smooth ⟨1-10⟩ side wall facets are seen. The top part of the wire (Fig.5.5 C) exhibits a stepped topography with a flat top surface arising during the final part of growth after TMIn has been switched off but the indium supply continues via surface diffusion for a short time. The top-view image in Fig.5.5 D shows the perfectly symmetric hexagonal shape of the wires.

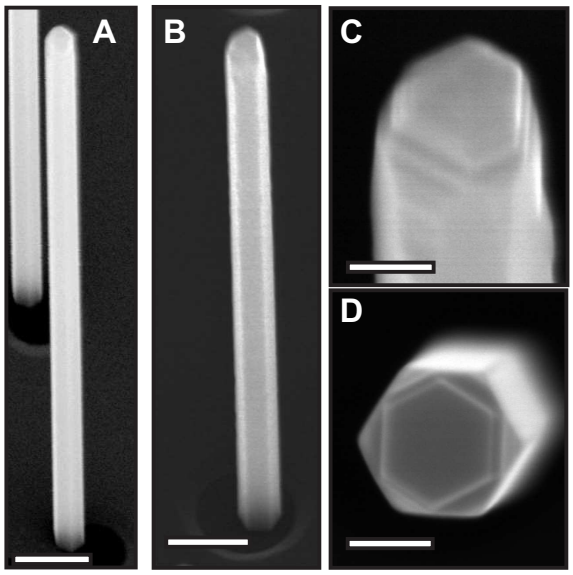


Figure 5.5: SEM pictures of Carbon- and Sulphur-doped InAs nanowires. **(A)** Carbon-doped nanowire revealing a slightly smaller diameter due to reduced nucleation. Scale bar is 200 nm. **(B)** No change in morphology or radial growth is observed for any sulphur concentrations used. Scale bar is 200 nm. **(C)** Close-up of the top of the wire. Scale bar is 50 nm. **(D)** Top view of the wire. Scale bar is 50 nm.

Doping with Si_2H_6

The same observations are made when using Si_2H_6 (Fig.5.6A) ; however, at $\Phi_{Si2H6}/(\Phi_{TMIn} + \Phi_{TBAs})$ ratios above 2×10^{-3} the ⟨111⟩ growth rate drops, whereas the ⟨1-10⟩ growth rate increases to several 10 nm/min. In addition, the side walls appear tapered (Fig.5.6B, C) because of the addition of critical amounts of Si atoms, which reduces the diffusion length of TMIn on the ⟨1-10⟩ surface. These effects become more pronounced with increasing $\Phi_{Si2H6}/(\Phi_{TMIn} +$

Φ_{TBAs}) ratios above 2×10^{-3}. Despite the tapered shape, the symmetric hexagonal shape of the wires is maintained as seen in Fig. 5.6.

A closer look into the crystal structure of undoped and doped nanowires reveals the same

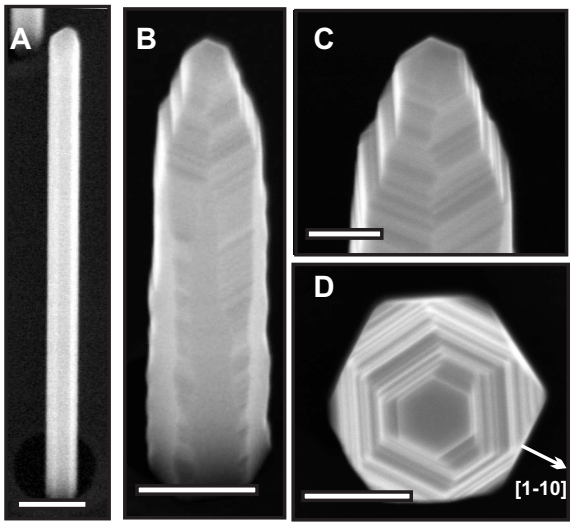


Figure 5.6: **(A)** For Si concentrations up to $\Phi_{Si2H6}/(\Phi_{TMIn}+\Phi_{TBAs}) = 2\times10^{-3}$, the nanowire morphology and radial growth are unchanged with respect to the undoped case. Scale bar is 200 nm. **(B)** Drastic changes in axial and radial growth as well as in morphology are observed for Si_2H_6 molar flows above $\Phi_{Si2H6}/(\Phi_{TMIn}+\Phi_{TBAs}) = 2\times10^{-3}$. Scale bar is 200 nm. **(C)** Close-up of the top of the tapered wire. Scale bar is 100 nm. **(D)** Top view of the wire. Scale bar is 100 nm.

crystal structure. No differences can be seen for all flow ratios and doping precursors. All InAs nanowires are zinc blende and exhibit stacking faults.

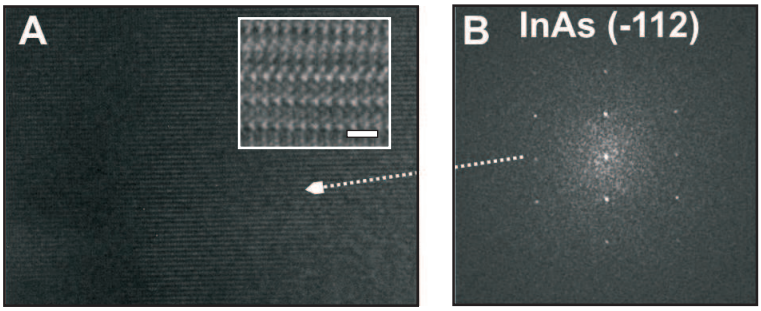


Figure 5.7: **(A)** TEM study of a Si doped InAs nanowire showing a zinc blende structure with stacking faults. Inset shows atomic periodicity of the crystal structure. Scale bar is 1.5 nm. **(B)** HR FFT picture depicting excellent periodicity of the crystal. *Courtesy: K. Reuter, F. Ross, IBM Yorktown*

5.2.2 Dopant Incorporation

To study the electrical properties of the C-, Si-, and S-doped InAs nanowires, two- and 4-point probe electrical measurements were performed as explained in the measurement chapter. The resistance is observed to increase linearly with nanowire length for all doping species, indicating a uniform conductance and therefore doping incorporation along the wire. As the wires are grown in very large arrays, radial growth is absent (for the conditions and doping species identified above) and hence no radial doping profile is expected. However, to exclude a radial doping profile, samples were thinned down ≈20–30 nm by wet chemical etching in a citric acid/peroxide ($C_6H_8O_7$:H_2O_2, 10:1) solution for 10–20s (Fig.5.8), after which the resistivity was measured once more. Fig.5.9 shows resistivity values before and after etching. The samples exhibited the same resistivity as before thinning, which indeed confirms a uniform radial dopant distribution.

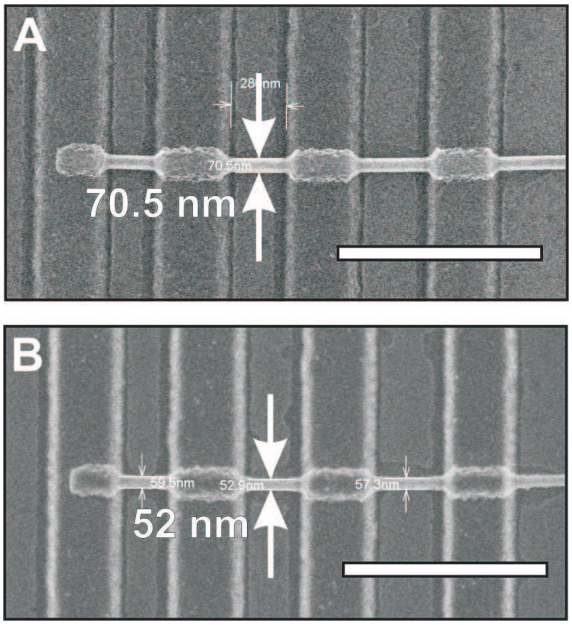


Figure 5.8: Resistivity Measurements before and after thinning down. **(A)** Measured silicon-doped InAs nanowire before thinning down. Scale bar is 1μm. **(B)** The same device after immersing it in a citric acid/peroxide wet chemical etching solution for 20s and measuring again. Scale bar is 1μm.

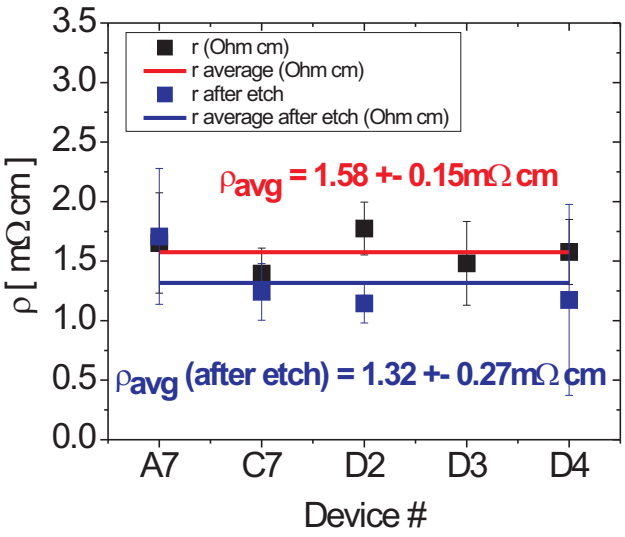


Figure 5.9: Measured resistivity of several silicon-doped InAs nanowires before and after thinning down. No significant change in resistivity is observed within the error bars. A slight trend to lower resistivity values after thinning down can be seen.

In Fig.5.10 the resistivity measured for various dopants is plotted vs. $\Phi_{Dop}/(\Phi_{TMIn}+\Phi_{TBAs})$. The resistivity of the non intentionally doped nanowires was measured to be 23 mΩcm but, as will be discussed later, this value does not correspond to the bulk resistivity in the wire. Carbon doping using CBr_4 at the maximum $\Phi_{CBr4}/(\Phi_{TMIn}+\Phi_{TBAs})$ ratio of 10^{-3} shows an increase in resistivity to 45 mΩcm indicating that C incorporates as a shallow acceptor. This is consistent with both the fact that carbon is a known amphoteric dopant in III/Vs and that at our conditions ⟨111⟩ growth is V-limited [BSB$^+$12] forcing incorporation on the As site. No further measurements using CBr_4 at reduced flows were conducted as no significant gain over Si and S doping was expected.

Employing Si_2H_6 doping instead, the nanowire resistivity was significantly reduced. A sharp decrease in resistivity with increasing Si_2H_6 concentration was observed (circular symbols in Fig. 5.10), yielding a minimum value of 0.26 mΩcm at $\Phi_{Si2H6}/(\Phi_{TMIn}+\Phi_{TBAs})= 2\times10^{-3}$, which is the highest ratio possible without changing morphology, as discussed previously. H_2S doping (lower curve with triangular symbols in Fig.5.10 shows a similar trend but reaches a minimum resistivity value of 0.6 mΩcm at $\Phi_{H2S}/(\Phi_{TMIn}+\Phi_{TBAs}) = 10^{-3}$, after which an increase in resistivity is observed.

The second curve for H_2S (upper curve with triangular symbols in Fig.5.10) is measured for

wires grown with identical V/III ratio, but at a TMIn flow of 0.95 μMol/min. The resistivity measured is overall higher than for the low TMIn molar flow data for all H_2S concentrations used. The difference between these two curves is attributed to a change in distribution coefficient of H_2S. In the inset of Fig.5.10 the axial growth rate, ν_{111}, is displayed as a function of TMIn flow [BSB$^+$12], showing two distinct regions corresponding to the conditions used for the two sulphur data sets in Fig.5.10. During growth in the high TMIn flow region (Φ_{TMIn} = 0.95 μMol/min), the V/III ratio is locally high, making sulphur incorporation (on the As site) less favorable because of a reduced distribution coefficient [Str89]. In the low TMIn flow regime (Φ_{TMIn} = 0.38 μMol/min), $\langle 111 \rangle$ growth is V-limited [BSB$^+$12], and in this case the local V/III ratio is lower than in the high TMIn flow regime. In the latter case, sulphur

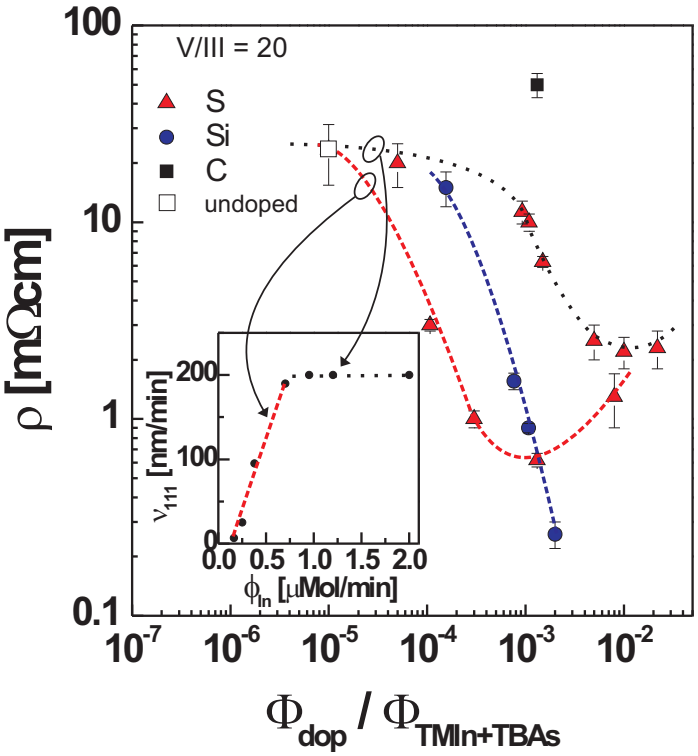


Figure 5.10: Doping incorporation. Measured resistivity of doped InAs nanowires vs. doping concentration in the gas phase for S (red symbols), Si (blue symbols), and C (black symbol) doping atoms. The dotted black curve shows the incorporation of S for a TMIn molar flow Φ_{TMIn} = 0.95 μMol/min, whereas the dashed red line shows the same for a TMIn molar flow Φ_{TMIn} = 0.38 μMol/min. The inset shows the axial growth rate as a function of TMIn flow, indicating two distinct regions of growth behavior corresponding to those identified in the main plot. The Si_2H_6 curve (dotted blue) exhibits no dependence on the TMIn molar flow.

incorporation therefore becomes more favorable (higher distribution coefficient). Such a dependence of the doping incorporation on the V/III ratio is also known, for example, from Zn doping of GaAs [KOKA92], [HMHK97]. Interestingly, the distribution coefficient of Si_2H_6 does not exhibit this dependence. Taking a closer look at the graph when the low TMIn flow data set for H_2S starts showing increasing resistivity values, also the high TMIn flow data set saturates. At high $\Phi_{H2S}/(\Phi_{TMIn} + \Phi_{TBAs})$ ratios, both curves seem to reach the same resistivity values. Because the minimum resistivity values of the two curves are dissimilar, it is unlikely that the ultimate increase in resistivity is due to auto-compensation driven by a lowering of the formation energy of native defects [Tok90], [Wal89], as this would always happen at a specific doping density (Fermi level position). Instead, it is assumed that at high sulphur to TMIn ratios, sulphur might form a complex in the host, which causes compensation[1] and thus an increase in the resistivity. The compensation effects are studied more closely in section 5.2.5 utilizing the Seebeck effect.

5.2.3 Establishing Doping Density and Mobility

Extracting doping densities and mobilities from the measured resistivity values is usually difficult because for each resistivity value two unknowns exist, the doping density N_D and carrier mobility μ_e. Common approaches use hall bar structures; but these are hard to build with single nanowires. A widely used method is to use the extracted transconductance from measured transistor transfer curves to calculate the field-effect mobility and carrier concentration in nanowires which has been shown using a backgate [DBR+07], a top gate [LSPW06] and a surround gate [BWFS06]. The main drawback is that for the extraction of mobility values requires the exact knowledge of the oxide capacitance C_{ox}. This is usually not known and very hard to measure in nanowire devices. Another issue is that parasitic contact, series and leakage resistances as well as capacitances from trap charges and interfaces have a significant impact on the calculations.

In order to circumvent this problem the doping concentrations of the nanowires here were extracted from the measured resistivity values by using three reference measurements without the need to approximate a mobility value.

[1] Compensation is referred here strictly as an increase in resistivity ρ

Doping Density Extraction by Seebeck Measurements

The first method consisted of measuring the Seebeck coefficient, S_T, of doped InAs nanowires [SMS+07]. It has been shown, both theoretically [Rod71] and experimentally [KMN+70] that there is a universal relationship between the Seebeck coefficient S_T and doping concentration in InAs, independent of the nature of donor impurity. The bulk relationship between S_T and

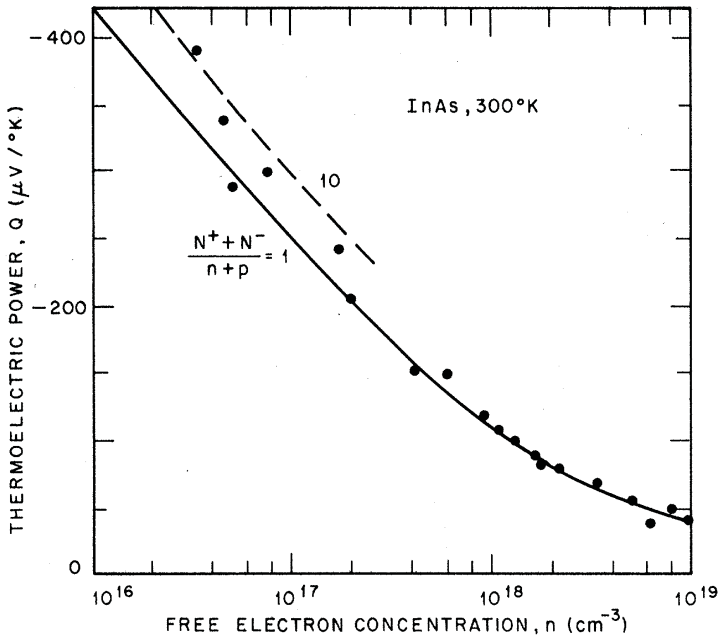


Figure 5.11: Seebeck coefficent as a function of bulk carrier concentration of InAs. After Rode, 1971, [Rod71].

N_D is shown in Fig.5.11 [Rod71]. The doping density is then be deduced for three different flow ratios during growth: $N_D = 4\times10^{18}$ and $N_D=1\times10^{18}$ cm^{-3} for $\Phi_{H2S}/(\Phi_{TMIn} + \Phi_{TBAs}) = 10^{-4}$, 10^{-3} (at high TMIn flow) and $N_D=7\times10^{19}$ cm^{-3} for $\Phi_{Si2H6}/(\Phi_{TMIn} + \Phi_{TBAs}) = 2\times10^{-3}$. Using the measured resistivity of ρ = 0.26, 3 and 10 mΩcm, a carrier mobility of μ_e = 344, 520 and 625 cm^2/Vs can be extracted.

Doping Density Extraction by Modelling of InAs Homojunction Tunnel Diodes

The second reference method consisted of analysing an InAs homojunction tunnel diode. The diode is processed from a Si-doped InAs nanowire ($\Phi_{Si2H6}/(\Phi_{TMIn} + \Phi_{TBAs}) = 10^{-3}$) on a p-type doped InAs substrate ($N_A = 1\times10^{19}$ cm^{-3}), as explained in the processing chapter. The electrical characteristic of such a diode is shown in Fig.5.12 as a function of temperature.

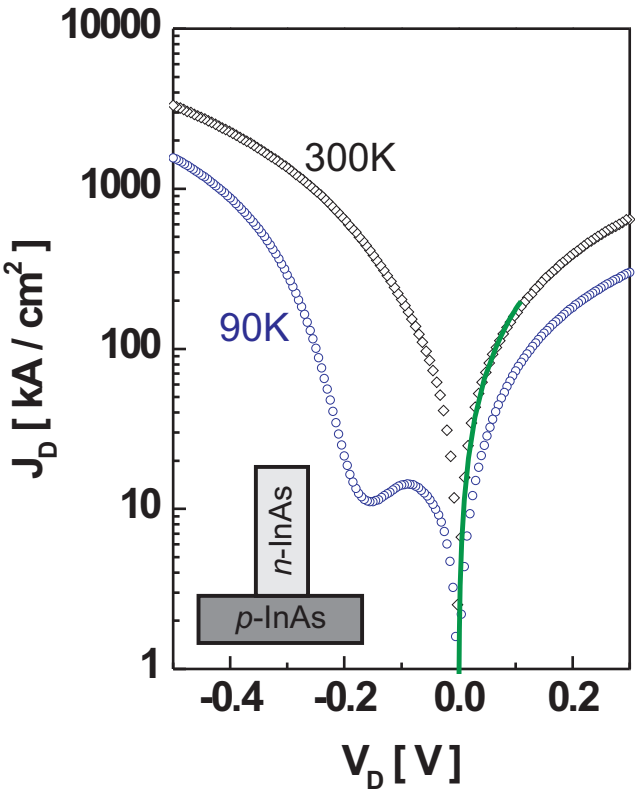


Figure 5.12: Vertical InAs homojunction Esaki diode. A negative differential resistance is observed at low temperature (blue symbols). At room temperature (black symbols) the reverse current density (positive voltage) reaches ≈ 300 kA/cm^2 at 0.3 V bias. TCAD modeling of these devices (solid line) were used to derive the doping density in the Si-doped InAs nanowire source region with a substrate doping $N_A = 1\times10^{19}$ cm^{-3}. The green line corresponds to the best fit with $N_D = 1\times10^{19}$ cm^{-3}.

Using TCAD simulations [SRLB11], it is possible to fit the characteristics to the experimental data for $N_D = 1\times10^{19}$ cm^{-3} (solid line in Fig.5.12). Using the measured resistivity of ρ = 1.6 mΩcm, a mobility of μ_e = 390 cm^2/Vs is extracted. [2]

Doping Density Extraction by Modelling of InAs Heterojunction Tunnel Diodes

The third reference method utilized was to fit the experimental data of an InAs/Si heterojunction tunnel diode [BSB$^+$11] using TCAD simulations [SRLB11] with the InAs nanowire doping concentration as the only fitting parameter.

[2] All TCAD simulations were done at ETH Zurich by Prof. Andreas Schenk.

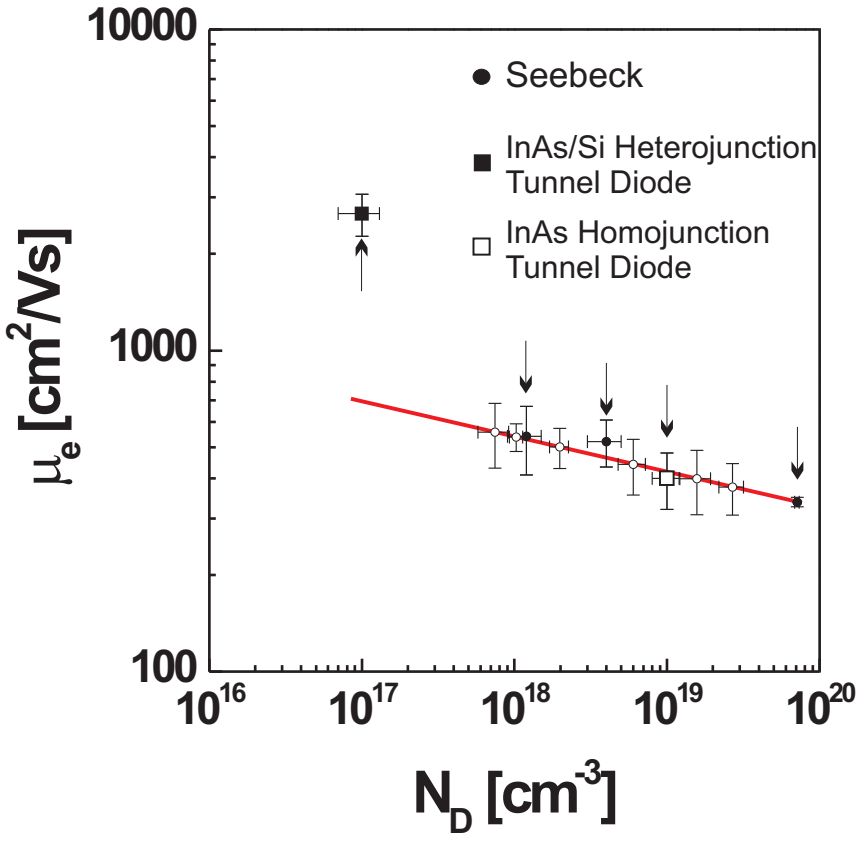


Figure 5.13: Electron mobility *vs.* doping density for InAs nanowires. The deviation from the dashed line at lower doping concentration is due to the inability to measure the resistivity correctly caused by the accumulation layer at the nanowire surface. Closed symbols are reference measurements and open symbols are extrapolated from the reference.

From that analysis, a doping concentration of $N_D = 1\times10^{17}$ cm^{-3} in undoped InAs nanowires was obtained. In Fig.5.13, the resulting carrier mobility vs. doping density is plotted for the nanowires with the five reference values indicated by filled symbols and black arrows. The mobility is observed to deviate from a linear trend only below $N_D = 1\times10^{18}$ cm^{-3}. This functional behavior is similar to the universal mobility dependence found in bulk InAs [KMRF77], and is also found for resistivity vs. doping density in Fig.5.14.

The plot in Fig. 5.14 was obtained by a line fit based on four reference values on which all resistivity measurements were overlaid to obtain the corresponding doping density values. Correspondingly, the open symbols in Fig.5.13 were calculated using the overlaid doping density values. The doping concentration can be thus controlled in the wires up to 7×10^{19} cm^{-3}, which is close to the maximum reported doping levels in bulk InAs [Sem78]. The deviation

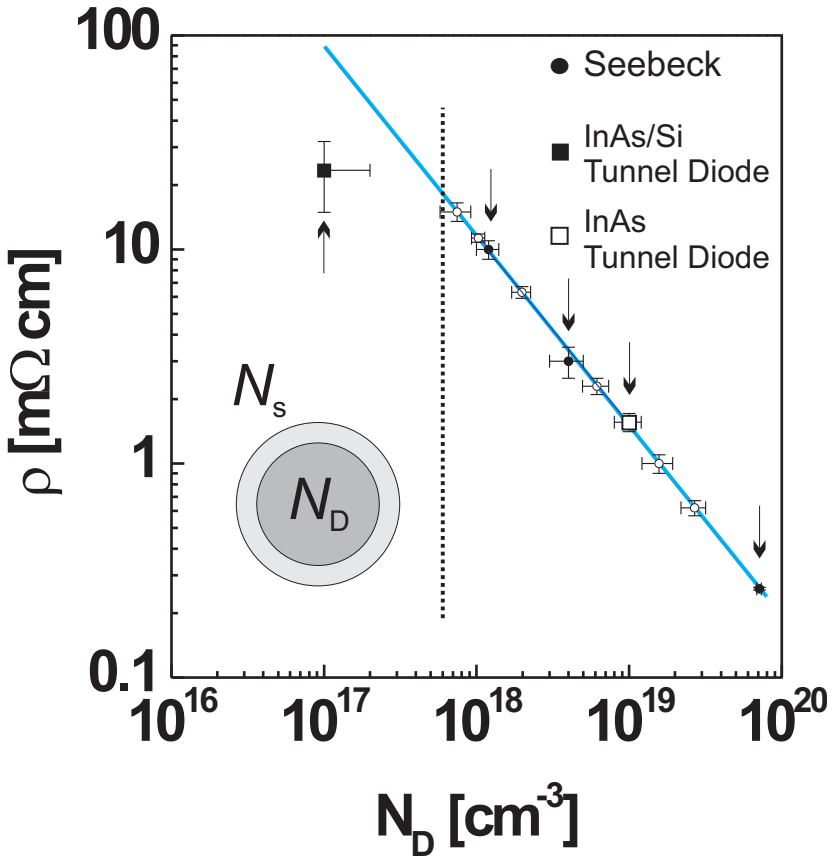


Figure 5.14: Resistivity vs. doping concentration for InAs nanowires. Below ND $\approx 8\times10^{17}$ cm^{-3} the measured resistivity is affected by the accumulation layer at the surface. By extrapolation a value for the resistivity of undoped nanowires of 60 mΩcm is determined, in contrast to the measured value of 23 mΩcm.

of resistivity for $N_D \leq 1\times10^{18}$ cm^{-3} from the trend at higher doping levels, results from an inhomogeneous carrier profile in the wire due to an accumulation layer [NHI91] at the surface, which prevents correct measurement of the resistivity. The accumulation layer formed on the ⟨1-10⟩ InAs surface typically has a sheet density $N_S \approx 1\times10^{12}$ cm^{-2} [CHL89] corresponding to a doping density of $\approx 8\times10^{17}$ cm^{-3} in a 10-nm-thick surface layer. A schematic of this effect is shown in Fig.5.15.

Based on the results shown in Fig.5.14 this doping density translates into a resistivity of 12 mΩcm, which is lower than that of the bulk part of the wire. The true resistivity in the bulk of the wire is obtained when extrapolating the data in Fig.5.14 to $N_D = 1\times10^{17}$ cm^{-3}, which yields ρ = 60 mΩcm. Alternatively, one can estimate the resistivity of the low-doped sample by accounting for the area of bulk resistivity in the core (100 nm in diameter with ρ = 60 mΩcm)

in parallel with an accumulation layer at the surface (10-nm-thick sheet with ρ = 12 mΩcm) to be ρ = 27 mΩcm, which is in good agreement with the measured value of ρ = 23 mΩcm. The existence of an accumulation layer at the surface is therefore the reason for the levelling off in the measured resistivity as the doping density drops below $\approx 1\times10^{18}$ cm^{-3}. Relating

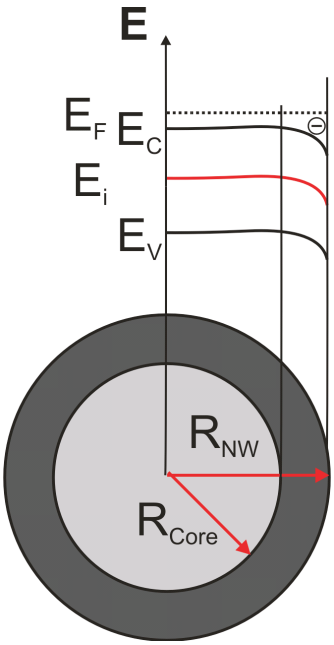


Figure 5.15: Schematics and band diagram of nanowire cross section depicting the accumulation layer present close to the InAs nanowire surface, leading to higher charge carrier densities close to the surface than in the core of the nanowire.

back to Fig.5.10, it is therefore not until a doping density of roughly 1×10^{18} cm^{-3} has been reached in the wire that a correct measurement of the resistivity becomes possible (uniform carrier profile is reached in the wire), and a drop in resistivity vs. $\Phi_{dop}/(\Phi_{TMIn}+\Phi_{TBAs})$ can be observed. The correct resistivity for undoped wires is thus ρ = 60 mΩcm, which is higher than those found for Au-catalyzed nanowires [TDB+10], but similar to values published by Wirths et al.[WWW+11]. The extracted resistivity for undoped nanowires corresponds to a doping density of 1×10^{17} cm^{-3} and a mobility of 1000 cm^2/Vs.

5.2.4 Contact Resistivity *vs.* Carrier Density

In addition to the resistivity, also the specific contact resisitivity was determined from the electrical measurements. This was done by plotting the measured resistivity values versus the electrode spacing, and determining the intercept of the linear curves with the resistance axis, as has been shown in the first part of this chapter. Fig. 5.16 displays the extracted contact resistivity as a function of doping concentration for Ti- and Ni-based contacts and fully alloyed Ni_xInAs nanowires. It is observed that the contact resistivity decreases by an order of magnitude with increasing doping concentration, from 1.2×10^{-6} Ωcm^{-2} for undoped nanowires to 1.7×10^{-7} Ωcm^{-2} for the highest doped nanowires. The Ni-based metallization schemes seem to give consistently lower contact resistivities than Ti-based schemes. In addition, the formation of a Ni alloy with InAs [CFH+08] has been shown to decreases the contact resistivity even further. The alloying process is done in a rapid thermal annealer (RTA) at 230°C for 2 min after the nanowires were contacted with thermally evaporated Ni contacts. The resistivity of the fully alloyed nanowires reaches a minimum value of 4×10^{-8} Ωcm^{-2}.

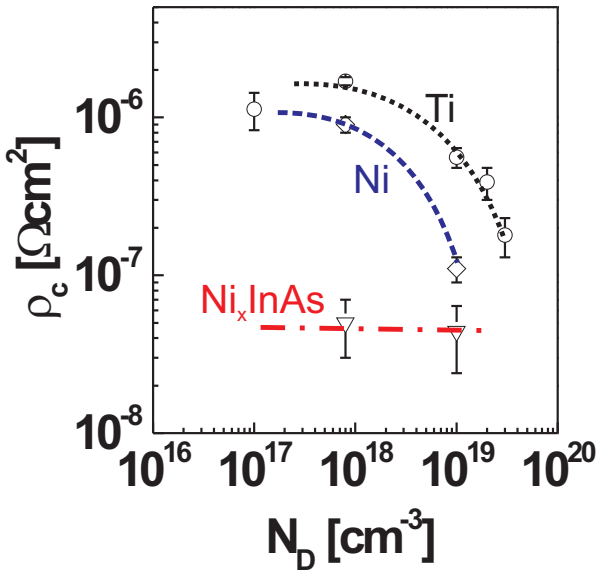


Figure 5.16: Contact resistivity vs. doping density for n-doped InAs nanowires. The topmost curve is for Ti contacts, the middle one for Ni contacts and the bottom one for fully alloyed Ni_xInAs nanowires.

5.2.5 Study of Compensation Effects by Seebeck Measurements

This section takes a closer look at the Sulphur doped InAs nanowires which showed compensation. As has been shown in Fig. 5.10 at higher $\Phi_{H2S}/(\Phi_{TMIn} + \Phi_{TBAs})$ flow ratios an increase in resistivity and thus, a decrease in doping densities was observed. As already pointed out in section 5.2.2 this compensation is likely to occur due sulphur complexes incorporating in the host InAs crystal at high sulphur to TMIn flow ratios.

There have been studies were compensation was observed, such as when doping with Zn in MOVPE grown GaAs [HMHK97] and in $Ga_{0.5}In_{0.5}P$ layers [KOKA92]. Another study by Foncuberta i Morral [KMUFiM10] showed that in MBE-grown GaAs nanowires Si can act as both a donor and acceptor. This behaviour appeared above a certain doping density of Si. The change from incorporation of Si at the As-site to the Ga-site was studied by Raman spectroscopy of the local vibrational mode and in the regime were compensation was present the formation of silicon pairs was observed [KMUFiM10]. The study also showed that the operating temperature during growth has an influence on the amphotericity of Si [DCG$^+$10].

Unlike Si in most III-V material, S is not amphoteric and the incorporation mechanism is more complex. The aim here is to study the influence that compensation has on the Seebeck coefficient and to get a clearer picture of the nature of the increase in resistivity.

The general form of the diffusive Seebeck coefficient for electrons is given by [PB10]:

$$S_T = \mp \frac{1}{eT}\left(\frac{\langle \tau E \rangle}{\langle \tau \rangle} - E_F\right) \tag{5.5}$$

where E_F is the Fermi energy and τ is the relaxation time or in other words, the time it takes for electrons to equilibrate through the effect of random scattering. The term $\langle \tau E \rangle$ is the average energy of electrons weighted by the relaxation time. As S_T is the difference of the weighted average energy of electrons and the Fermi energy, S_T can be interpreted as the tendency of electrons having an average energy E in a band to return to the lowest energy state which is represented by the Fermi energy E_F. The Seebeck coefficient decreases slightly with temperature and as E_F is increased. The main term which is responsible for an increase of S is $\langle \tau E \rangle$. The increase of electron scattering by ionized impurities or phonons increases the relaxation time which in turn leads to an increase in the weighted average energy. The relaxation time at a certain electron energy can be approximated by a power law of the form $\tau(E) = \tau_0(E - E_0)^r$. The scattering constant r increases when ionized impurity scattering is present and, thus the relaxation time increases. The existence of scattering centers can therefore increase the

Seebeck coefficient.

For the experiment, the same batch of Sulphur doped InAs nanowires as used in section 5.2.2 were measured and the Seebeck coefficient was extracted. The measurement procedure is described in Appendix A.6. The nanowires exhibiting compensation as shown in Fig.5.10 and uncompensated nanowires which had approximately the same resistivity as the compensated ones were considered. This was to elucidate whether having the same measured resistivity a difference in the Seebeck coefficient can be seen. The measured Seebeck coefficient as a function of flow ratio during growth is shown in Fig.5.17. The Seebeck coefficient of the lowest Si doped nanowires is also shown in blue circles. The dotted black and dashed red curve represents the Sulphur doped nanowires grown at high and low TMIn flow, respectively. At high $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ ratios (all three red triangular points to the right of the vertical dotted line in Fig.5.17) an increase in the Seebeck coefficient is observed which is also observed for the resistivity in Fig.5.10. A slightly different trend can be seen when the measured Seebeck coefficients are plotted against the extracted doping density. Fig.5.18 shows the extracted

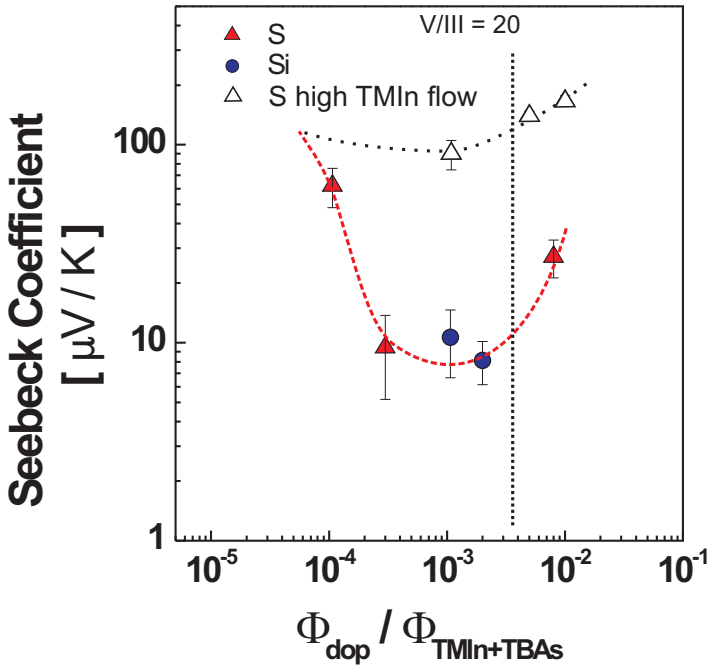


Figure 5.17: Measured Seebeck coefficient vs. $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ flow ratio for S and Si doped InAs nanowires. At high $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ ratios an increase in the Seebeck coefficient is seen for Sulphur doped InAs nanowires.

doping concentration with associated Seebeck coefficients. The red dashed line corresponds to the bulk relation between carrier concentration and Seebeck coefficient as depicted in Fig.5.11. It can be seen that all Seebeck coefficients of Sulphur doped nanowires grown at low TMIn flow agree well with the bulk relationship. This is also the case for the compensated Sulphur doped nanowire (red triangular point on red dashed line third from the left) which was grown at low TMIn flow. In the case of both compensated Sulphur doped samples grown at high TMIn flow (topmost points which are circled in Fig.5.18) the Seebeck coefficient deviates from the bulk relationship. This is depicted by the black dotted line which is a guide to the eye. The sample exhibit Seebeck coefficients of 140μV/K and 166μV/K which is roughly an increase of almost 2.5 compared with the bulk relation of carrier density to Seebeck coefficient.

Thus, Sulphur doped nanowires grown at high TMIn flow show an enhanced Seebeck coeffi-

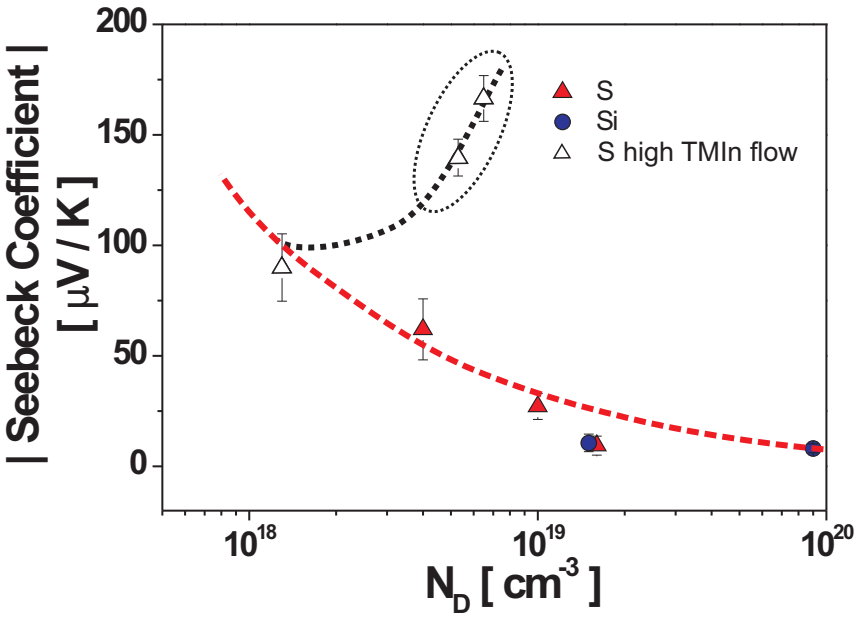


Figure 5.18: Measured Seebeck coefficient vs. doping density. the red dashed line corresponds to the bulk relationship between Seebeck coefficient and carrier concentration for n-doped InAs. The experimental Seebeck coefficients fit well the bulk relationship for Si doped InAs nanowires and S doped nanowires grown at a low TMIn flow. For S doped nanowires grown at high TMIn flow an increase in the Seebeck coefficient of about 2.5 is observed.

cient. The nature of compensation and Seebeck enhancement is likely to stem from Sulphur complexes which are formed during nanowire growth as the $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ is increased. This compensation seems to appear only at high TMIn flow and thus when the V/III

ratio is locally high [BSB+12]. At a high local V/III ratio Sulphur incorporation is less favourable as has been shown by Bjoerk et al. [BSB+12], and as the $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ is increased the formation and incorporation of Sulphur complexes can happen at vacancies and other defect sites. As an increase in active impurity dopants would also increase the Fermi level and decrease the Seebeck coefficient, it is more likely that Sulphur complexes which do not affect the carrier density leads to an increase in the Seebeck coefficient. These complexes don't add any further active carriers but rather act as charged impurities which increase the overall scattering of electrons. This then leads to an increase in weighted average energy and thus, a higher Seebeck coefficient.

The above experimental results show that an enhancement of the Seebeck coefficient is seen when InAs nanowires are doped with Sulphur to the extent that compensation of charge carriers is observed. The origin of compensation is believed to stem from charged Sulphur complexes in the InAs crystal which lead to an increase in the scattering rate of carriers. There are, however, more experiments needed to verify these assumptions. Further studies of the crystal structure of compensated doped nanowires is anticipated as well as Raman studies.

5.2.6 Summary

The following table summarizes the parameters used for InAs nanowire growth such as dopant precursors, TMIn flow and $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ ratio during growth, measured resistivity values and extracted doping density N_D as well as carrier mobility μ. Doping incorporation can be controlled from $1{\cdot}10^{17}$ cm^{-3} to $7.1{\cdot}10^{19}$ cm^{-3} with mobility values ranging from 2670 down to 337 cm^2/Vs. Furthermore, Seebeck coefficients S are listed. The Seebeck coefficients of samples which didn't show compensation agree well with the bulk relation of S and N_D in InAs. As for compensated samples where an increase in resistivity with increasing flow ratio $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ was observed the Seebeck coefficient revealed a 2.5-fold increase compared with the bulk relation of carrier density to Seebeck coefficient. It is assumed that the origin of compensation stems from charged Sulphur complexes in the InAs crystal which lead to an increase in the scattering rate of carriers and thus, an increase in the Seebeck coefficient. Further measurements to elucidate the nature of the Sulphur complexes could make use of Raman studies measuring the local vibrational modes associated with sulphur in the crystal.

Table 5.1: Summary of Parameters for Growth and Experimental Data

Impurity	**Flow Ratio**	**TMIn Flow** [μMol/min]	ρ [mΩcm]	μ [cm^2/Vs]	**N**$_D$ [cm^{-3}]	S_T [μV/K]
non-int.	-	0.38	23.4±8	2670±400	$1{\cdot}10^{17}$	166±4
CBr_4	$1{\cdot}10^{-3}$	0.38	50±7	-	-	-
Si_2H_6	$1.5{\cdot}10^{-4}$	0.38	15±7	557± 126	$7.5{\pm}1.7{\cdot}10^{17}$	-
Si_2H_6	$7.6{\cdot}10^{-4}$	0.38	1.56±0.15	400±80	$1{\pm}0.2\cdot10^{19}$	-
Si_2H_6	$2{\cdot}10^{-3}$	0.95	0.9±0.05	399±90	$1.6{\pm}0.4\cdot10^{19}$	10.6±4
Si_2H_6	$1{\cdot}10^{-3}$	0.38	0.26±0.04	337±11	$7.1{\pm}0.2\cdot10^{19}$	8±2
H_2S	$1.07{\cdot}10^{-4}$	0.38	3±0.2	520±86	$4{\pm}1\cdot10^{18}$	62±13
H_2S	$3{\cdot}10^{-4}$	0.38	1±0.1	540±130	$1.2{\pm}0.2\cdot10^{18}$	-
H_2S	$1.31{\cdot}10^{-3}$	0.38	0.62±0.05	375±65	$2.7{\pm}0.5\cdot10^{19}$	9.5±4
H_2S	$8{\cdot}10^{-3}$	0.38	1.3±0.4	-	-	27±6
H_2S	$5{\cdot}10^{-5}$	0.95	2.5±0.5	-	-	-
H_2S	$9.29{\cdot}10^{-4}$	0.95	11.3±1.5	538±53	$1{\pm}0.1\cdot10^{18}$	90±15
H_2S	$1.09{\cdot}10^{-3}$	0.95	10±1	-	-	-
H_2S	$1.5{\cdot}10^{-3}$	0.95	6.3±0.4	500±70	$2{\pm}0.3\cdot10^{18}$	-
H_2S	$5{\cdot}10^{-3}$	0.95	2.5±0.5	-	-	140±8
H_2S	$1{\cdot}10^{-2}$	0.95	2.2±0.4	442±85	$6.1{\pm}1.2\cdot10^{18}$	166±10
H_2S	$2.2{\cdot}10^{-2}$	0.95	2.3±0.5	-	-	-

5.3 InAs Homojunction Tunnel Diodes

This section describes the experimental results of InAs homojunction tunnel diodes. Single tunnel diodes were processed as described in the Device Fabrication chapter. The diodes were processed from a Si-doped InAs nanowire with a doping density of N_D=1×10^{19}cm^{-3} on a p-type doped InAs substrate (N_A=1×10^{19}cm^{-3}). Experimental data of some diodes were used as well for establishing the doping density with TCAD modeling as described earlier in section 5.2.3. The aim here though is to record $I-V$ curves at low temperatures to obtain temperature dependent tunnel diode characteristics and determine tunneling current densities as well as peak-to-valley current ratios (PVCR). The need to go to low temperature is that at room temperature the dominating current of an InAs homojunction is thermionic current due to the small bandgap of InAs. It is therefore only when going to low temperatures that the tunnel and valley current appear. In order to confirm that BTBT is present and the dominant current a temperature sweep is done. The $I-V$ characteristics of two single homojunction tunnel diodes are shown in Fig. 5.19 AS expected at room and high temperature no NDR is observed in forward direction (here at negavtive V_D). Going to lower temperatures in forward direction (negavtive V_D), the current is decreased at lower temperatures, which is mainly due to the

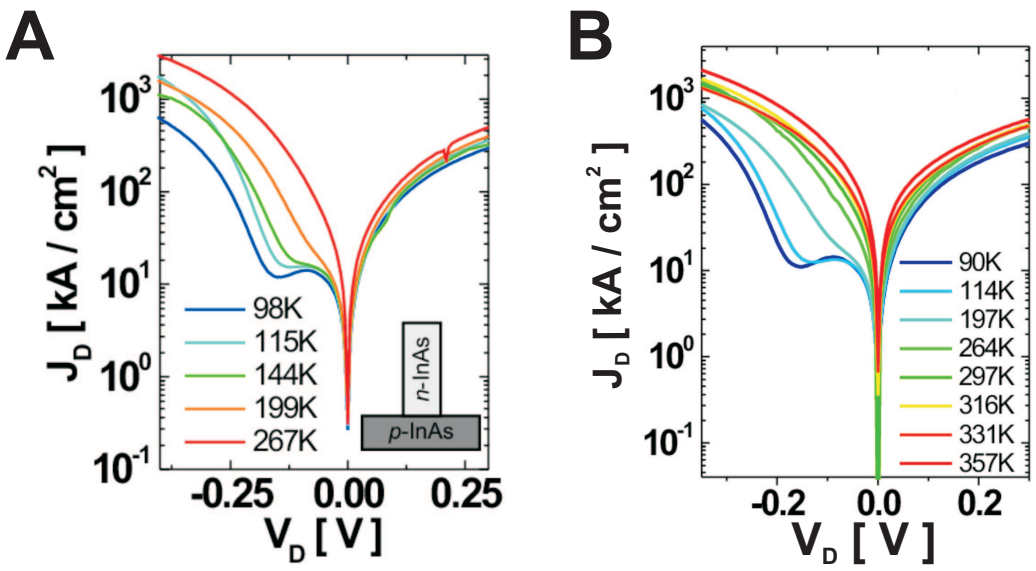


Figure 5.19: Temperature dependent $I-V$ characteristics of two InAs homojunction tunnel diodes:

presence of a series resistance. This could stem from the contacts to the nanowire or the nanowire itself. Going below 200K the valley current becomes visible and as the temperature is lowered even more the valley gets more pronounced. Around 100 mV forward bias at the peak of valley current, where the energetic window for direct tunneling disappears, only tunneling via trap states remains and increases the excess current as discussed in section 1.4.1. Both the peak and valley currents vary with temperature, with a trend that the current increases with increasing temperature. This leads to a reduced peak-to-valley current ratio at higher temperatures. The maximum obtained PVCR is about 1.4 which is roughly the same for all devices measured. Current densities at room temperature were obtained showing current densities in the range of 500kA/cm^2 at 0.3V reverse bias.

5.4 Summary

This chapter presented first a doping study of InAs nanowires. Different n-type doping precursors were utilized and doping incorporation ranging from $1{\cdot}10^{17}$ cm^{-3} to $7.1{\cdot}10^{19}$ cm^{-3} was achieved which is comparable to the highest doping concentration reported in bulk InAs. These doping densities are achieved without changes in the morphology or the radial growth, and are uniform, both axially and radially in the nanowires. For very high doping flows of Si_2H_6, the radial growth and the morphology change drastically for increasing doping concentration in the gas phase. A new method utilizing the bulk relation of the Seebeck coefficient and carrier density was used to extract doping concentrations without assuming a mobility value. Two other reference methods were utilized were TCAD simulations are fitted to the electrical characteristics of a *p-n* InAs homojunction diode as well as a InAs-on-Si heterjunction tunnel diode. From the the fitted *I-V* curves a doping density and mobility can be extracted.
When using sulfur as a dopant, compensation effects occurred at very high concentrations. The compensated samples where an increase in resistivity with increasing flow ratio $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ was observed show an increase of the Seebeck coefficient by 2.5 compared with the bulk relation of carrier density to Seebeck coefficient. It is assumed that the origin of compensation stems from charged Sulphur complexes in the InAs crystal which lead to an increase in the scattering rate of carriers and thus, an increase in the Seebeck coefficient.
The specific contact resistivity is shown to decreas by an order of magnitude with increasing doping concentration from $1.5{\cdot}10^{-6}$ Ωcm^{-2} for undoped nanowires to $1.7{\cdot}10^{-7}$ Ωcm^{-2} for the highest doped ones and Ni-based metallization schemes give lower contact resistivity than Ti-based schemes.
InAs homojunction tunnel diodes were fabricated and electrically characterized. Temperature dependent measurements revealed typical NDR behaviour belowe 200 K. The maximum obtained PVCR was about 1.4 and current densities in the range of 500 kA/cm^2 at 0.3 V reverse bias at room temperature were observed.

The results demonstrate the possibility to achieve very high doping densities in in-situ doped grown InAs nanowire structures and high tunneling currents in InAs homojunction tunnel diode. It is anticipated that an increase in n-type doping densities will lead to higher on-currents in the InAs-on-Si heterostructure Tunnel FETs shown so far by our group.

6 Conclusions

The work presented in this thesis focused on bottom-up fabricated nanowire Tunnel devices on a Si platform. To achieve this lateral Si Tunnel FETs, vertical FETs and doping in InAs for implementation in heterostructure Tunnel FETs were studied. First, single lateral Si nanowire Tunnel FETs grown by the vapor-liquid-solid method (VLS) were fabricated and electrically characterized. Device parameters were extracted and the influence of a HfO_2 gate dielectric on the device performance was studied. A process flow for vertical Si FET devices was developed and processing issues were investigated and solutions were provided, leading to a new improved fabrication process. First vertical Si nanowire FETs were presented. *In-situ* doping of InAs nanowires grown by selective area epitaxy in a MOVPE tool was thoroughly investigated. The effect of various group-IV and group-VI doping species on nanowire morphology, axial and radial growth rates, as well as electrical properties was studied. A method utilizing the measured Seebeck coefficient to extract doping densities without the need of assuming a mobility value was shown to give accurate doping denisities. Two other reference methods where *I-V* characteristics of homo-and heterojunction InAs tunnel diodes are fitted by TCAD simulations confirmed this approach. Furthermore, first vertical tunnel diodes based on n-doped InAs nanowires grown on p-InAs substrates were electrically characterized.

The main achievements in this work are summarized in the following:

Performance enhancement of lateral Si Tunnel FETs by a high-κ gate dielectric

Si Tunneling FETs with an in-situ p-i-n^+ doping profile were fabricated and electrically characterized. Electrical characterization of p-n and p-i-n diodes showed good ideality factors $\eta \approx 2$. The junction abruptness of the i-n^+ junction was measured to be between 7.5 nm and 30 nm per decade of carrier concentration. Two different gate stacks for Tunnel FETs, namely 20 nm SiO_2 and 5 nm HfO_2 were investigated. The device having the strongest gate coupling (5 nm HfO_2) exhibited the highest I_{on} of ≈0.1 μA/μm at V_{DS}=0.5 V which is a 4-fold increase as compared to the sample with SiO_2 and on par with other reported Si-based Tunnel FETs. It exhibited the steepest average $S \approx 120$ mV/dec over 4 decades as compared with the SiO_2 gate stack, combined with an I_{on}/I_{off} ratio on the order of 10^6. The S value only went below the 60mV/dec limit at very low voltages which is likely due to non-ideal abruptness of the i-n^+ junction. However, the average values are improved as compared to literature. Temperature-dependent measurements were carried out, showing a non-ideal behaviour, and it was demonstrated by later studies of our group that this was due to a potential barrier at the p-type segment caused by the Ti/Au contact. The barrier was removed when a Ni/Au contact metallization was used. This potential barrier may well have limited the I_{on} of the tunnel FETs.

Development of a vertical process for bottom-up nanowire FETs

A full vertical process for Si nanowire FETs was developed. The process is easily adaptable to other materials such as InAs. A big issue during processing was the presence of Au residues stemming from the VLS-growth of Si nanowires. In particular, Au catalyses reactions in the presence of BHF which leads to the etching of Si. Another issue observed was the antenna effect during etching of the BCB or polyimide layer in an RIE tool. Appearing craters were removed by spin coating a second highly diluted BCB layer to fill up the craters. With these improvements a new process was then presented. However, the yield of working vertical devices is still very low, something which is being tackled as the vertical process is the basis for the ongoing development of vertical InAs on Si Tunnel FETs in our group.

Doping study of InAs nanowires and Realization of InAs homojunction Tunnel diodes

Different n-type doping precursors such as Si_2H_6, H_2S, DETe and CBr_4 were utilized and doping incorporation ranging from $1{\cdot}10^{17}$ cm^{-3} to $7.1{\cdot}10^{19}$ cm^{-3} was achieved which is comparable to the highest doping concentration reported in bulk InAs. The highest doping density was reached with Si doping. The doping densities were achieved without changes in the morphology or the radial growth, and are uniform, both axially and radially in the nanowires. The addition of the slightest amount of DETe completely inhibits ⟨111⟩ growth and only ⟨1-10⟩ growth is possible, making DETe non-suitable for in-situ doping of nanowires unless pure shell doping is needed. A new method utilizing the bulk relation of the Seebeck coefficient and carrier density was used to extract doping concentrations without assuming a mobility value. Two other reference methods were utilized. This included fitting the electrical characteristics of a *p-n* InAs homojunction diode as well as a InAs-on-Si heterojunction tunnel diode with TCAD simulations. From the fitted *I-V* curves a doping density and mobility was then extracted. The mobility values ranged from 442 for the highest doped sample to 2670 cm^2/Vs for undoped InAs nanowires.
InAs homojunction tunnel diodes were fabricated by growing *in-situ*-Si doped InAs nanowires on *p*-InAs substrates. Temperature-dependent measurements revealed typical negative differential resistance (NDR) behaviour below 200 K. The maximum obtained peak current to valley ratio (PVCR) was about 1.4 and very high reverse current densities in the range of 500 kA/cm^2 at 0.3 V reverse bias at room temperature were observed. The obtained doping densities are promising to boost the on-current of InAs-on-Si Tunnel FETs which are currently fabricated in our group.

Enhancement of Seebeck coefficients in compensated sulfur-doped InAs nanowires

Compensation effects occurred at very high Sulphur concentrations in InAs nanowires. The compensated samples where an increase in resistivity with increasing flow ratio $\Phi_{Dop}/(\Phi_{TMIn} + \Phi_{TBAs})$ was observed show an increase of the Seebeck coefficient by 2.5 compared with the bulk relation of carrier density to Seebeck coefficient. Although generally unwanted in materials, we showed that compensation of free carriers leads to enhanced Seebeck coefficients. This is an important finding when considering the application of InAs nanowires for thermoelectric energy generation where a high Seebeck coefficient is needed to achieve high

ZT values, the thermoelectric figure of merit. It is assumed that the origin of compensation stems from charged Sulphur complexes in the InAs crystal which lead to an increase in the scattering rate of carriers and thus, an increase in the Seebeck coefficient.

6.1 Future Work

The Si material system has the benefit of easy integration with conventional CMOS technology. Additionally, the nanowire geometry offers the ideal wrap-gate architecture. The all-Si Tunnel FETs presented in this thesis achieved similar device performance as planar Ge-based Tunnel FETs which was shown by an internal study at IBM Research and indicates the benefits of the nanowire geometry. Future work could include the reduction of the nanowire diameter and gate oxide thickness to further enhance the gate coupling as well as improving the junction abruptness to lower the inverse subthreshold slope.

A limiting factor for Si based Tunnel FETs is the low on-current. To obtain higher on-currents by increasing the tunnel probability at the source-channel tunnel junction a lower bandgap source material is employed. By only changing the source material one maintains the advantage of Si as channel, drain and substrate material which is preferable due to the low interface state density of Si and the achievable high I_{ON}/I_{OFF} ratios. Additionally, the vertical process introduced here allows for the gate to completely wrap around the channel.

The control of doping density in the InAs source material enables further engineering of tunneld barrier width at the tunneling junction. Also, maintaining high enough doping densities in the top contact area of InAs-on-Si Tunnel FETs reduces the series resistance and hence further boosts the on-current. Although not yet experimentally shown, simulations indicate that InAs-on-Si heterostructure Tunnel FETs can exhibit high on-currents.

As for the vertical process flow, there are several improvements to be made to reduce process variability and increase the yield. Process variability mainly occurs when etching down the gate or the BCB spacer layer. The RIE etch parameters also have to be adjusted according to the nanowire material used. Alongside with the ongoing work in our group in fabricating InAs-on-Si Tunnel FET the use of a high-κ gate dielectric can be considered. Investigation into the effect of traps at the heterojunction interface on device performance needs to be conducted.

The choice to grow III-V material by MOVPE on Si substrates allows easier integration and the use of common VLSI technology as compared to utilizing solely III-V materials. This could be an important factor when considering future implementation. As for complementary Tunnel FETs a three-material system including InAs, Si and Ge is considered to have potential as both InAs and Ge can be integrated on Si subtrates.

Further detailed studies on the compensation effects in InAs nanowires are being explored. Raman studies measuring the local vibrational modes associated with sulphur and comparing

compensated nanowires with ones which do not show compensation could shed some more light into the nature of compensation. Understanding the reason for the Seebeck coefficient enhancement could lead to further interesting studies on how to boost the ZT value of InAs nanowires which is of importance for energy harvesting applications.

A Appendix

A.1 Details on InAs Nanowire MOVPE Growth Process

The crystal growth processes themselves occuring during MOVPE growth are very complex and the precise description of the process is out of scope for this thesis. This section gives a more detailed overview on MOVPE growth of InAs nanowires. The main process is explained as follows: A gas mixture containing the precursors needed for growth, and if necessary for doping, is passed over a heated substrate. The chemical effect occuring at the substrate is pyrolysis of the precursors, i.e. the chemical decompostion of metalorganic and hydride compounds by heat in the absence of oxygen. Homogeneous reactions in the gas phase in the boundary layer and heterogeneous reactions on the substrate surface or reactor walls are the two dominating reactions where the latter one occurs more at lower temperatures. The vapor phase is the main phase supplying the growth material. However, precursors which have a low vapor pressure can also contribute to the growth via surface diffusion. Compared to molecular beam or chemical beam epitaxy the gas flow in MOVPE is viscous, that is molecules are strongly interacting at a base pressure of >50 Torr [Str89]. The main components are shown in Fig. A.1. The precursors used here are group-III metalorganics (MO), MO dopants, group-V hydrides and hydride dopants. All metalorganic and group-V precursors are liquid at room temperature and are stored in bubblers where H_2 is injected into the bubbler "carrying" the precursor through the gas lines into the injector block and subsequently into the reaction chamber. The flow rate of each line is controlled by flow controllers. Alkyl and Hydride precursors are inserted through separate injector blocks to inhibit chemical reactions between the two before entering the reaction chamber. The actual mixing of all reagents takes place

within the reaction chamber. To achieve uniform mixing each precursor line is split up into 3 lines entering the chamber at different positions (for simplicity Fig. A.1 shows only one entrance into the chamber). The growth substrate sits on a heated sample holder and is rotated to minimize temperature gradients across the substrate as well as to enhance the precursor mixing. The main pump attached to the chamber is in constant operation allowing a continues flow over the substrate. After the gas mixture leaves the reaction chamber it is put through a scrubber before it reaches the exhaust.

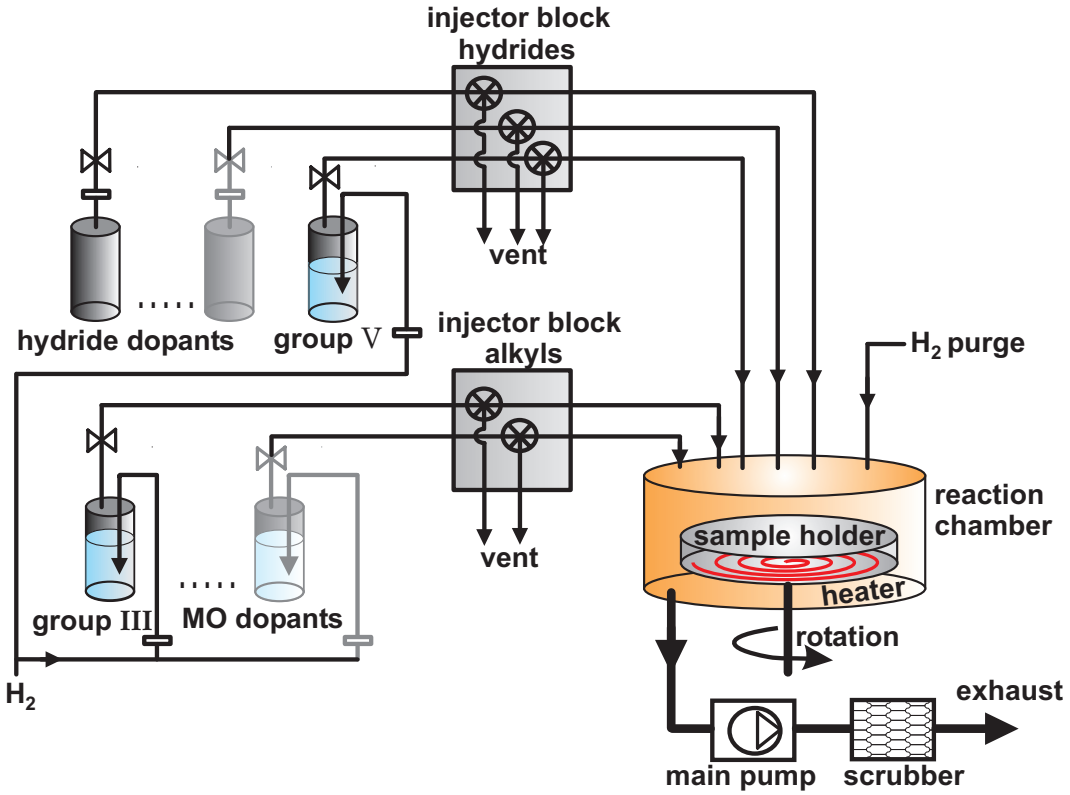


Figure A.1: Schematic illustration of a MOVPE system

A.2 Run Card for Lateral Si Tunnel FET

Step	Process Description	Parameters
	Photolitho for Pads:	
1	HMDS	15 s, 3000 rpm
2	Resist spinning N415	4000 rpm, 40 s, bake 3 min, 90°C
3	UV-Exposure	75 s, vacuum contact
4	Development	M32 1'40"
5	O_2-Plasma clean	200 W, 30 s within cage
6	metal deposition	Ti/Au 3 nm / 60 nm
7	Lift-off in Acetone	
8	spin PMMA for protection during cleaving	
9	remove protective resist	Acetone + IPA
10	O_2-Plasma clean	200 W, 60 s no cage
	NW deposition	
11	dry transfer	pin wires
	Detect NW coordinates - optical	
12	light microscope	to avoid charging of wires
13	mask design (two levels: gate, contacts)	
	Gate dielectric	
14	PECVD oxide deposition	20 nm
	Gate metalization	
15	PMMA 950k, 4% Anisol	1300 rpm, 40 s
16	Bake Hot Plate	180°C, 90"
17	verify resist thickness by scratching	dektak 350 nm
	e-beam exposure (gate)	
18	Raith e-beam tool	175 μC/cm^2, 20 kV, Ap=10 μm, WF=100 μm
19	develop: (IPA:H_2O) (7:3)	50 s, no ultrasound, blow dry
20	O_2-Plasma clean	150 W, 30 s in cage
21	metal deposition	Aluminium 120 nm
22	Lift-off in Acetone	(rinse in IPA)
	Contact lithography	
23	O_2-Plasma clean	200 W, 30 s no cage
24	PMMA 950k, 4% Anisol	1300 rpm, 40 s Gyrset
25	Bake Hot Plate	180°C, 90 s
26	free alignment marks	

Continued on next page.

Step	Process Description	Parameters
	e-beam exposure (contacts)	
27	Raith e-beam tool	175 μC/cm^2, 20kV, Ap=10 μm, WF=100 μm
28	develop: IPA:H2O (7:3)	50 s No ultrasound
29	O_2-Plasma clean	150 W, 15 s within cage
30	BHF dip	22 s
31	immediately load in evaporation chamber	
32	metal deposition	Ti/ Au 8 nm / 11 nm
33	Lift-off in Acetone	+rinse in IPA
34	O_2-Plasma clean	150 W, 15 s within cage
35	BHF dip	10 s
36	immediately load in evaporation chamber	
37	metal deposition	Ti/ Al, 10 nm / 110 nm
38	Lift-off in Acetone	+ rinse in IPA

A.3 Run Card for Lateral Si Tunnel FET with HfO_2 Dielectric

Step	Process Description	Parameters
	Photolitho for Pads:	
1	HMDS	15 s, 3000 rpm
2	Resist spinning N415	4000 rpm, 40 s, bake 3 min, 90°C
3	UV-Exposure	75 s, vacuum contact
4	Development	M32 1'40"
5	O_2-Plasma clean	200 W, 30 s within cage
6	metal deposition	Ti/Au 3 nm / 60 nm
7	Lift-off in Acetone	
8	spin PMMA for protection during cleaving	
9	remove protective resist	Acetone + IPA
10	O_2-Plasma clean	200 W, 60 s no cage
	NW deposition	
11	dry transfer	pin wires
	Detect NW coordinates - optical	
12	light microscope	to avoid charging of wires
13	mask design (two levels: gate, contacts)	
	Gate dielectric	
14	ALD Hafnium dioxide deposition	5 nm
	Gate metalization	
15	PMMA 950k, 4% Anisol	1300 rpm, 40 s
16	Bake Hot Plate	180°C, 90"
17	verify resist thickness by scratching	dektak 350 nm
	e-beam exposure (gate)	
18	Raith e-beam tool	175 $\mu C/cm^2$, 20 kV, Ap=10 μm, WF=100 μm
19	develop: (IPA:H2O) (7:3)	50 s no ultrasound, blow dry
20	O_2-Plasma clean	150 W, 30 s in cage
21	metal deposition	Ti/Au 10 nm / 110 nm
22	Lift-off in Acetone	(rinse in IPA)
	HfO2 etch	
23	0.5% HF in H_2O	60 s

Continued on next page.

Step	Process Description	Parameters
24	**Isolation PECVD SiO_2**	30 nm 300°C
	Contact lithography and Gate Opening	
25	O_2-Plasma clean	200 W, 30 s no cage
26	PMMA 950k, 4% Anisol	1300 rpm, 40 s Gyrset
27	Bake Hot Plate	180°C, 90 s
28	free alignment marks	
	e-beam exposure (contacts)	
29	Raith e-beam tool	175 μC/cm^2, 20 kV, Ap=10 μm, WF=100 μm
30	develop: IPA:H2O (7:3)	50 s No ultrasound
31	O_2-Plasma clean	150 W, 15 s within cage
32	BHF dip	22 s
33	immediately load in evaporation chamber	
34	metal deposition	Ti/ Au 8 nm / 110 nm
35	Lift-off in Acetone	(rinse in IPA)

A.4 Run Card for Vertical Si FETs

Step	Process Description	Parameters
	Nanowire Growth	
1	Random Growth	60 nm Au colloids, n+ or p+ Si wafer
2	**Au Removal**	short HF:H_2O (1:5) dip, 30 s in KI/I_2
3	rinse in DI	
	Preparation for Doping Top Part	
4	Field oxide	PECVD SiO_2 100 nm
5	HMDS	3000 rpm, 15 s
6	Resist spinning AZ 6612	1500 rpm, 40 s
7	Bake Hot Plate	110°C, 1'
8	verify resist thickness by scratching	dektak 2.1 μm
9	RIE etch of resist	O_2 plasma, resist height 700 nm
10	BHF(1:10) etch of top	50-60s
11	resist strip	immediately, Aceton, rinse in IPA
	OPTION 1: Diffusion Doping	
12.a1	Phosporous doped SiO_2	PECVD 20 nm
12.a2	Capping Oxide	SiO_2 PECVD 40 nm
12.a3	Drive-in Anneal	RTA, 950°C 60 s Ar
12.a4	Resist strip	HF(1:4) 30 s
	OPTION 2: Implantation	
12.b1	Boron	dose:$4.5{\cdot}10^{14}$cm^{-2}, 45° angle
12.b2	strip off field oxide	BHF(1:10), 2'30 s
12.b3	Activation anneal	RTA, 1000°C 10 s H_2/Ar
	Isolation of NWs	
	Mesa Photolitho	
13	HMDS	15 s, 3000 rpm
14	Resist spinning N415	4000 rpm, 40 s, bake 3', 90°C
15	UV exposure	75 s, vaccum contact
16	Development	M32, 1'40"
17	O_2-Plasma clean	200 W, 30s within cage
18	remove native oxide	BHF 5 s
	Mesa etch	
19	isotropic RIE SF_6/Ar	100:100 sccm, 150 mTorr, 40 W, 1'
20	resist strip	Acetone, rinse in IPA
21	O_2 plasma clean	RIE tool, 100 mTorr, 2'
	Vertical etch	
22	RIE etch SF_6/Teflon	40:70 sccm, 1200 W, 10 s, 130 nm
23	O_2 plasma clean	RIE tool, 100 mTorr, 2'
24	BHF dip	10 s, SEM inspection

Continued on next page.

Step	Process Description	Parameters
	Field Isolation	
25	Field oxide	PECVD SiO_2 100 nm
	Litho for holes	
26	HMDS	15 s, 3000 rpm
27	Resist spinning AZ6612	1500 rpm, 40 s
28	Bake Hot Plate	110°C, 1'
29	UV-Exposure	8 s, vacuum contact
30	Development	400K (1:4) 22 s
31	O_2-Plasma clean	200 W, 20 s within cage
32	Etch holes into field oxide	BHF 1:10, 64 s
33	strip resist	Acetone, rinse in IPA
	Gate dielectric	
34	PECVD oxide deposition	20 nm
	Gate metalization	
35	Sputtering	Al, 100 nm
	Gate length definition	
36	HMDS	3000 rpm, 15 s
37	Resist spinning AZ 6612	1500 rpm, 40 s
38	Bake Hot Plate	110°C, 1'
39	verify resist thickness by scratching	dektak 2.1 μm
40	RIE etch of resist	O_2 plasma, resist height 800 nm
41	BHF dip	5 s
42	Al gate metal etch	phosp.-/nitr.acid/H_2O (85/5/10vol-%), 84 s
50	resist strip	immediate Acetone, rinse in IPA
43	O_2-Plasma clean	200 W, 20 s on top of cage
	Photolitho for gate pads	
44	HMDS	15 s, 3000 rpm
45	Resist spinning N415	4000 rpm, 40 s, bake 3 min, 90°C
46	UV-Exposure	75 s, vacuum contact
47	Development	M32 1'40"
48	O_2-Plasma clean	200 W, 30 s within cage
49	Al etch	85 s
50	resist strip	Acetone, rinse in IPA

Continued on next page.

Step	Process Description	Parameters
	Spacer layer	
51.a1	OPTION 1: Polyimide	
51.a2	HD Adhesion	3000 rpm, 1' 120°C
51.a3	PI 5878G diluted 2:1	2000 rpm, 4' 135°C
51.a4	Hard bake	200°C for 30' –> 350°C for 1 h, N_2
51.a5	RIE etch of Polyimide	O_2 plasma
51.a6	verify resist thickness by scratching	dektak 1 μm
51.b1	OPTION 2: BCB	
51.b1	AP3000 and BCB	undiluted 4000 rpm
51.b2	Hard bake	250°C, Ar, 10 min
51.b3	RIE etch of BCB	SF_6/O_2 plasma (5/50 sccm), 25 W
51.b4	verify resist thickness by scratching	dektak 1 μm
	Top contact	
52	Litho for contacts	
53	HMDS	15 s, 3000 rpm
54	Resist spinning AZ6612	1500 rpm, 40 s
55	Bake Hot Plate	110°C, 1'
56	UV-Exposure	8 s, vacuum contact
57	Development	400K (1:4) 22 s
58	O_2-Plasma clean	200 W, 20 s within cage
	BHF dip	22 s
59	immediately load in evaporation chamber	
60	metal sputtering	Ti/ Au 10 nm / 100 nm
61	Lift-off in Acetone	(rinse in IPA)
	Back contact	
62	metal evaporation	Ti/ Au 10 nm / 100 nm
	Opening to gate pad	
63	Litho for contacts	
64	HMDS	15 s, 3000 rpm
65	Resist spinning AZ6612	1500 rpm, 40 s
66	Bake Hot Plate	110°C, 1'
67	UV-Exposure	8 s, vacuum contact
68	Development	400K (1:4) 22 s
69a1.	OPTION 1: Polyimide	
69.a2	RIE etch of Polyimide	O_2 plasma
69.b1	OPTION 2: BCB	
69.b2	RIE etch of BCB	SF_6/O_2 plasma (5/50 sccm), 25 W
70	resist strip	Acetone, rinse in IPA

A.5 Run Card for Improved Process for Vertical Si FETs

Step	Process Description	Parameters
	Intrinsic MBE layer	
1	MBE growth of Si	150 nm, on n^+-Si 111 wafer
2	Random Growth	60 nm Au colloids, n-type nanowires
3	**Au Removal**	short HF:H_2O (1:5) dip, 30 s in KI/I_2
4	rinse in DI	
	Vertical etch: MBE and into wafer	
5	RIE etch SF_6/Teflon	40:70 sccm, 1200 W, 1', 130 nm
6	O_2 plasma clean	RIE tool, 100 mTorr, 2'
7	BHF dip	10 s, SEM inspection
	Isolation of NWs	
8	Mesa Photolitho	
9	HMDS	15 s, 3000 rpm
10	Resist spinning N415	4000 rpm, 40 s, bake 3', 90°C
11	UV exposure	75 s, vaccum contact
12	Development	M32, 1'40"
13	O_2-Plasma clean	200 W, 30 s within cage
14	remove native oxide	BHF 5 s
	Mesa etch	
15	isotropic RIE SF_6/Ar	100:100 sccm, 150 mTorr, 40 W,1'
16	resist strip	Acetone, rinse in IPA
17	O_2 plasma clean	RIE tool, 100 mTorr, 2'
	Field Isolation	
18	Field oxide	PECVD SiO_2 100 nm
	Litho for holes	
19	HMDS	15 s, 3000 rpm
20	Resist spinning AZ6612	1500 rpm, 40 s
21	Bake Hot Plate	110°C, 1'
22	UV-Exposure	8 s, vacuum contact
23	Development	400K (1:4) 22 s
24	O_2-Plasma clean	200 W, 20 s within cage
25	Etch holes into field oxide	BHF 1:10, 64 s
26	strip resist	Acetone, rinse in IPA
	BCB isolation bottom	
27	AP3000 and BCB	undiluted 4000 rpm
28	Hard bake	250°C, Ar, 10 min
29	RIE etch of BCB	SF_6/O_2 plasma (5/50 sccm), 25 W
30	verify resist thickness by scratching	dektak 1 μm
31	2nd BCB layer to fill craters	diluted 1:20, 2000 rpm
32	RIE etch of BCB	SF_6/O_2 plasma (5/50s ccm), 25 W, 1'40"

Continued on next page.

Step	Process Description	Parameters
	Gate dielectric	
33	PECVD oxide deposition	20 nm
	Gate metalization	
34	Sputtering	Al, 100 nm
	Gate length definition	
35	HMDS	3000 rpm, 15 s
36	Resist spinning AZ 6612	1500 rpm, 40 s
37	Bake Hot Plate	110°C, 1'
38	verify resist thickness by scratching	dektak 2.1 μm
39	RIE etch of resist	O_2 plasma, resist height 800 nm
40	BHF dip	5 s
41	Al gate metal etch	phosp.-/nitr.acid/H_2O (85/5/10 vol-%), 84 s
42	resist strip	immediate Acetone, rinse in IPA
43	O_2-Plasma clean	200 W, 20 s on top of cage
	Photolitho for gate pads	
44	HMDS	15 s, 3000 rpm
45	Resist spinning N415	4000 rpm, 40 s, bake 3 min, 90°C
46	UV-Exposure	75 s, vacuum contact
47	Development	M32 1'40"
48	O_2-Plasma clean	200 W, 30 s within cage
49	Al etch	85 s
50	resist strip	Acetone, rinse in IPA
	BCB spacer layer	
51	AP3000 and BCB	undiluted 4000 rpm
52	Hard bake	250°C, Ar, 10 min
53	RIE etch of BCB	SF_6/O_2 plasma (5/50 sccm), 25 W
54	verify resist thickness by scratching	dektak 1 μm
55	2nd BCB layer to fill craters	diluted 1:20, 2000 rpm
56	RIE etch of BCB	SF_6/O_2 plasma (5/50 sccm), 25 W, 1'40"
	Top contact	
57	Litho for contacts	
58	HMDS	15 s, 3000 rpm
59	Resist spinning AZ6612	1500 rpm, 40 s
60	Bake Hot Plate	110°C, 1'
61	UV-Exposure	8 s, vacuum contact
62	Development	400K (1:4) 22 s
63	O_2-Plasma clean	200 W, 20 s within cage

Continued on next page.

Step	Process Description	Parameters
64	BHF dip	22 s
65	immediately load in evaporation chamber	
66	metal sputtering	Ti/ Au 10 nm / 100 nm
67	Lift-off in Acetone	(rinse in IPA)
	Back contact	
62	metal evaporation	Ti/ Au 10 nm / 100 nm
	Opening to gate pad	
63	Litho for contacts	
64	HMDS	15 s, 3000 rpm
65	Resist spinning AZ6612	1500 rpm, 40 s
66	Bake Hot Plate	110°C, 1'
67	UV-Exposure	8 s, vacuum contact
68	Development	400K (1:4) 22 s
69a1.	OPTION 1: Polyimide	
69.a2	RIE etch of Polyimide	O_2 plasma
69.b1	OPTION 2: BCB	
69.b2	RIE etch of BCB	SF_6/O_2 plasma (5/50 sccm), 25 W
70	resist strip	Acetone, rinse in IPA

A.6 Seebeck Measurements

This section gives an overview on Seebeck measurements of InAs nanowires, experimental setup and the method to extract doping densities from the measured Seebeck coefficient. The setup is part of the Thermoelectrics activity in our group and was build up by Dr. Siegfried Karg and Philipp Mensch. It was their original design for contacting nanowires for Seebeck measurements which was used throughout the experiments [Men].

Thermoelectric materials have gained tremendous interest over the last decade due to their capability to convert heat into electricity through the Seebeck effect. When given a heat source and a sink heat can be transferred either through the motion of carriers or through collective lattice vibration modes/phonons. The carrier transport results in a potential difference which is called the Seebeck voltage ΔV_S. The universal description of how big a potential difference can be generated by a temperature difference between heat source and sink ΔT is given by the Seebeck coefficient $S_T = \Delta V_S / \Delta T$. As explained in chapter 5 the universal relationship between the Seebeck coefficient S and doping concentration for direct-gap materials such as InAs can be utilized to extract doping densities by measuring the Seebeck voltage between in a nanowire. This relationship is independent of doping species and can be applied over the entire doping concentration range [Rod71], [KMN$^+$70].

To measure a Seebeck voltage along a nanowire a heat source has to be placed at one end

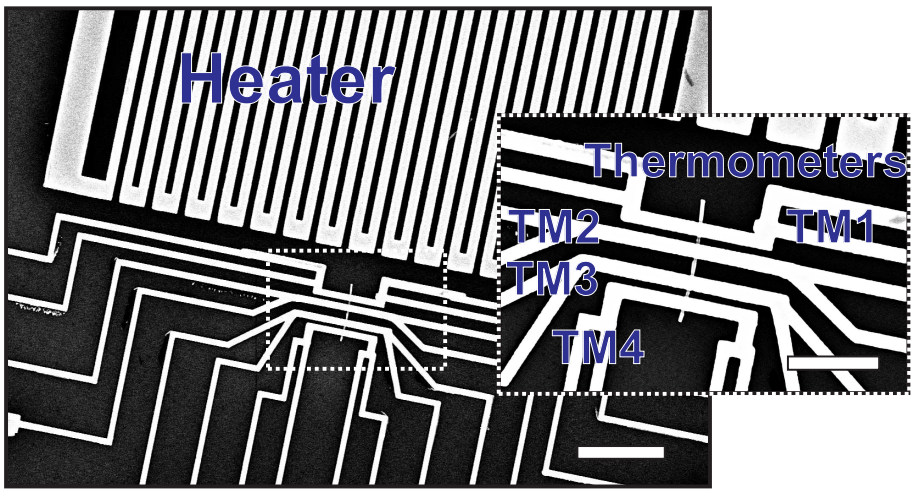


Figure A.2: SEM image of a contacted InAs nanowire device for Seebeck Measurements. Meander heater and thermometers, labelled as TMs, are fabricated by ebeam lithography and lift-off. Scale bar is 5 μm, in inset 2μm.

of the nanowire allowing for heat flow to the cooler side at the other end of the nanowire.

The heat source in our case is a metallic meander structure fabricated by ebeam lithography and lift-off on a Si substrate covered by 100 nm of SiO_2. To heat the area around the heater a current is run through it. The Seebeck voltage is measured by contacting the nanowire electrically, again by ebeam lithography and lift-off, and measuring the voltage drop between two contacts to the nanowire. These contacts are referred to as "thermometers". Typically, 4 contacts are made to each nanowire. 20 nm Ti, of which the first 10 nm are evaporated under a 45^{deg} tilt, followed by 140 nm Pt evaporation serve as contact metal for both the heater and thermometers. An SEM image of a fabricated device can be seen in Fig A.2 where the meander heater is located close to an end of the InAs nanowire. The inset shows a close up of all thermometers, labelled as "TM", and the nanowire. Each thermometer has 4 leads which are connected to contacting pads and enables accurate resistance extraction of each contact lead by 4-point probe. The heater has 4 outgoing leads to contact pads as well.

The sample is mounted on a coldfinger in a flow cryostat. A Probe card with probe needles is placed over the device of interest and aligned manually. In this way all pads of the device are each contacted with one probe at the same time when the probe card is lowered down towards sample (see chapter 3). The probe card is connected to a Keithley 707 Switching matrix outside of the cryostat which in turn assigns each prober to either a Keithley 6221 current source, a digital multimeter, a 6517A electrometer or a 2182A nanovoltmeter. All instruments are connected through GPIB with a desktop computer and a automated Labview program, written by Dr. Siegfried Karg, which controls the instruments and the cryostat heater and cooling valve for liquid nitrogen.

To measure the Seebeck voltage along the nanowire a voltage is applied over the meander heater, heating the area around it. Two thermometers are connected to a nanovoltmeter measuring the Seebeck voltage along the nanowire at different heating voltages. The Seebeck voltage is shown in Fig.A.3 as a function of heating voltage, depicting the characteristic parabola-shape. To elucidate what the real temperature difference is between the two thermometers, first the resistance of both thermometers has to be measured as a function of heating voltage. This is done by measuring the 4-point probe resistance through the 4 contact leads to one thermometer to exclude any contact resistance. A certain resistance is then associated to each heating voltage value. The next step is to calibrate the thermometers from a given resistivity value to an exact temperature value. For this, the sample is heated from 298 K to 312 K in the cryostat and at each temperature interval the 4-point probe resistance

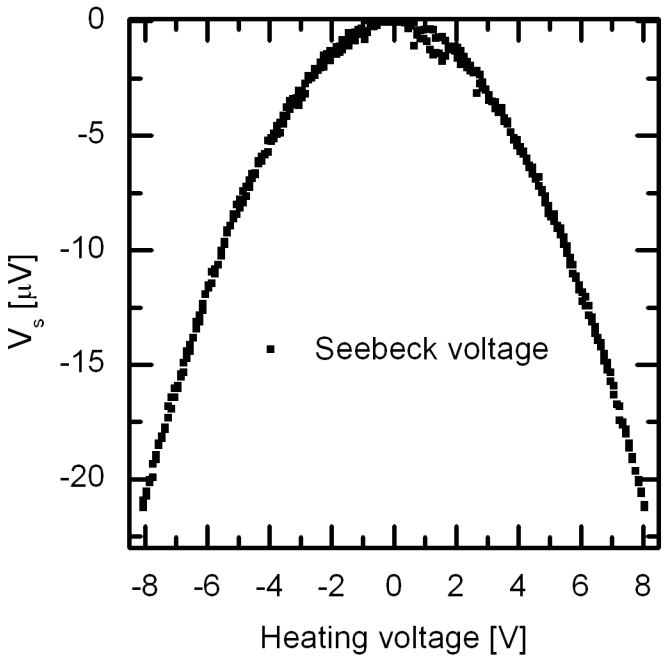


Figure A.3: Seebeck voltage as a function of heating voltage.

is measured of both thermometers. This gives a linear relationship beteween temperature and %-change in resistance as illustrated in Fig.A.4. The parameter %-change in resistance is utilized here since different thermometers have a different resistance but in general the same %-change in resistance as they are fabricated from the same metal. For Pt and Ti the temperature range from 250 to 350 is always linear so that the same %-change in resistance is valid for our experiments. Having now the %-change in resistance as a function of temperature, the change in resistance of the thermometer when sweeping the heating voltage can be translated into a temperature difference as shown in Fig.A.5 A: at a given heating voltage each thermometer shows a different temperature and thus a different temperature difference, as one is closer to the heater than the other.

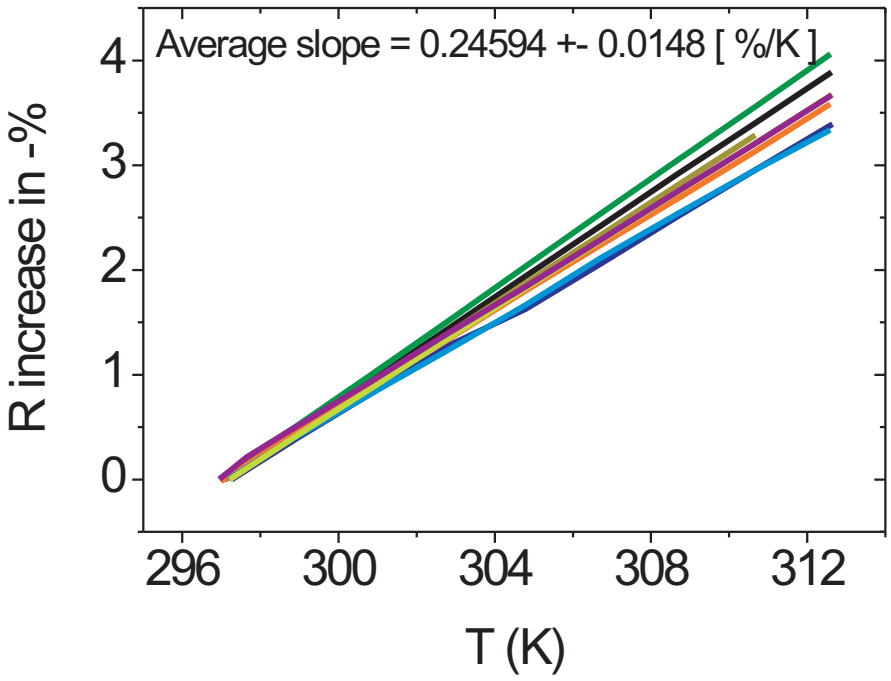


Figure A.4: %-Resistance increase as a function of temperature for different thermometers of different devices.

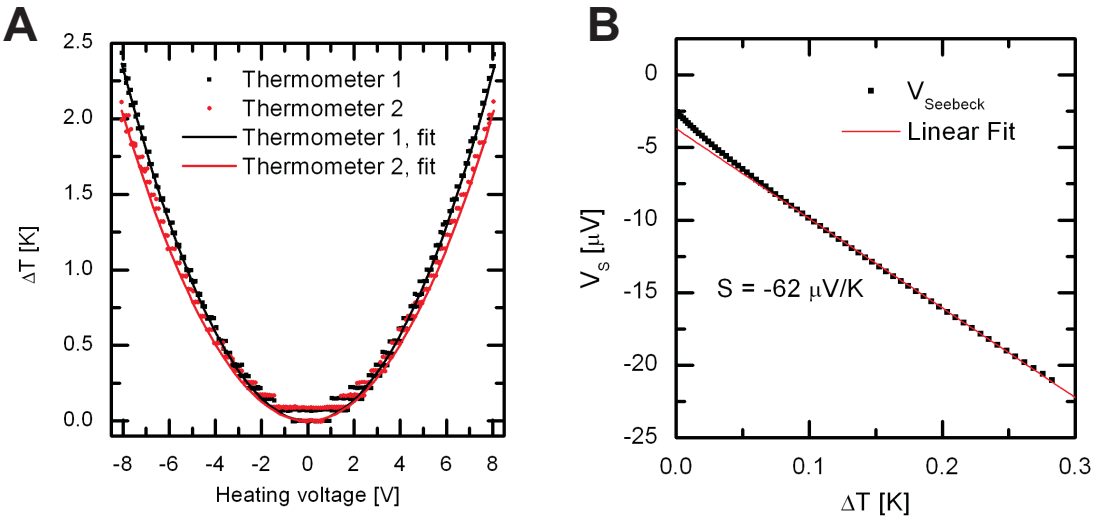


Figure A.5: Extraction of Seebeck coefficient: **(A)** Temperature difference ΔT of two thermometers, contacting the same nanowire at different positions relative to the heater, as a function of heating voltage. **(B)**Plotting the measured Seebeck voltage as a function of relative temperature difference between the same two thermometers, which were used to measure the Seebeck voltage, reveals a slope which is equal to the Seebeck coefficient.

A.7 List of technical acronyms

Acronym	Description
ALD	atomic layer deposition
BHF	buffered hydrofluoric acid (HF)
CMOS	complementary metal-oxide-semiconductor
CVD	chemical vapour deposition
DG	double gate
DI	dionized water
DIBL	drain-induced barrier lowering
DI	dionized water
FD-SOI	fully depleted silicon-on-insulator
FET	field effect transistor
GAA	gate-all-around
ITRS	international technology roadmap for semiconductors
MEMS	micro electro-mechanical systems
MOSFET	metal-oxide-semiconductor field effect transistor
PECVD	plasma enhanced CVD
PD-SOI	partially depleted silicon-on-insulator
SEC	short channel effects
SEM	scanning electron microscopy
SOI	silicon-on-insulator
TCAD	technology computer aided design
TEM	transmission electron microscopy
ZT	figure of merrit in thermoelectrics

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Pressure is nothing more than the shadow of great opportunity.

Michael Johnson

List of publications and presentations

H. Ghoneim, P. Mensch, H. Schmid, C. Bessire, R. Rhyner, A.s Schenk, C. Rettner, S. Karg, K. Moselund, H. Riel and M. Björk, "In-situ Doping of Catalyst-free InAs Nanowires", *submitted to Journal of Applied Physics*, 2012.

S. Karg, P. Mensch, B. Gotsmann, H. Schmid, P. Das Kanungo, H. Ghoneim, V. Schmidt, M. Björk, V. Troncale, and H. Riel, "Measurement of thermoelectric properties of semiconductor nanowires", *31st International and 10th European Conference on Thermoelectrics*, July 9th-12th, Aalborg, Denmark, 2012.

H. Ghoneim, P. Mensch, H. Schmid, C. Bessire, S. Karg, K. Moselund, H. Riel and M. Björk, "In-situ Doping of Catalyst-free InAs Nanowires", *MRS Fall Meeting*, 28th Nov – 2nd Dec 2011, Boston, USA, 2011.

H. Schmid, K.E. Moselund, M.T. Björk, M. Richter, H. Ghoneim, C.D. Bessire, and H. Riel. "Fabrication of vertical InAs-Si heterojunction tunnel field effect transistors". In *Device Research Conference (DRC)*, 2011 69th Annual, pages 181 –182, 2011.

K.E.Moselund, M.T. Björk, H. Schmid, H. Ghoneim, S. Karg, E. Lortscher, Walter Riess, and H. Riel. "Silicon nanowire tunnel fets: Low-temperature operation and influence of high-κ gate dielectric", *IEEE Transactions on Electron Devices*, 58(9):2911–2916, 2011.

H. Schmid, K.E. Moselund, M.T. Björk, M. Richter, H. Ghoneim, C.D. Bessire and H. Riel, "Fabrication of vertical InAs-Si heterojunction tunnel field effect transistors", *Proc. IEEE 69th Annual DRC*, Santa Barbara, Ca, 2011.

M. T. Björk, H. Schmid, C. D. Bessire, K. E. Moselund, H. Ghoneim, S. Karg, E. Lörtscher, and H. Riel, "Si–InAs heterojunction Esaki tunnel diodes with high current densities", *Applied Physics Letters*, 97, 163501, 2010.

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H. Ghoneim, K. E. Moselund, M. Björk, H. Schmid, S. Karg, D. Webb, M. Tschudy, R. Beyeler and H. Riel, "Doping of VLS-grown Silicon Nanowires for FETs" *Deutsche Physikalische Gesellschaft Spring Meeting*, Regensburg, Germany, 2010.

K. E. Moselund, H. Ghoneim, H. Schmid, M. T. Björk, E. Lörtscher, S. Karg, G.Signorello, D. Webb, M. Tschudy, R. Beyeler and H. Riel, "Solid-state diffusion as an efficient doping method for silicon nanowires and nanowire field effect transistors", *Nanotechnology*, 21, 435202, 2010.

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PERSONAL INFORMATION

- **Date of birth:** November 9th, 1983
- **Place of birth:** Riyadh, Saudi Arabia
- **Nationality:** Austrian, Egyptian

WORK EXPERIENCE

IBM Research-Zurich, Switzerland (Nov. 2008 – present)
Pre-doctoral Researcher – Nanoelectronics for post-CMOS

- **Nanowire-based steep-slope devices** on Si platforms for possible low-power applications.
- **Established significant experience in nanotechnology and sub-micron CMOS processing** such as cleanroom work, Ebeam lithography, dry/wet etching, thin films, microstructure electrical characterization (low temperature, DC/AC, vacuum systems, SEM, AFM, spectroscopy).
- **Elected co-president** of pre-doctoral candidates at IBM Research.

Humatica, Switzerland (Jan. 2008 – Oct. 2008)
Analyst in Management Consulting/ Corporate Strategy

- **Established and completed a strategy plan** for a global metering company combining **energy management, energy efficiency, smart grid technologies and smart metering**.

Import Business for Mobile Accessories (2005-2006)
Founder

- **Successfully created an import distribution channel** for solar-powered cell phone chargers in Egypt with direct distribution to medium-sized retailers.

EDUCATION

Swiss Federal Institute of Technology (EPF Lausanne, Switzerland) (2009 – present)
Doctor of Philosophy in Microsystems and Microelectronics (completion Fall 2012)

- **Investigation of** Si Nanowire Tunnel FETs, the route towards heterostructure Tunnel FETs on a Si platform, the as well as technological challenges to achieve these device structures.

Swiss Federal Institute of Technology (ETH Zurich, Switzerland) (2002 – 2008)
Bachelor and Masters in Interdisciplinary Natural Sciences
Major: Solid State Physics and Physical Chemistry, Minor: Molecular Biology and Biophysics

- **Developed methods** for interface engineering for Metal-Semiconductor contact optimization in Silicon Nanoelectronics.

University of Salzburg, Austria (2001 – 2002)

- **Studies of Applied Computer Sciences during** high school through a scholarship from the Austrian Center for the Promotion of Gifted Students.

LANGUAGES

English (native), **German** (native), **Arabic** (fluent), **French** (fluent), **Spanish** (proficient)

INTERESTS

Track and Field, Flamenco Guitar, Scuba Diving